# VLSI Labs 1&2

## Simple MOSFET & CMOS Inverter Trends

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### I. Introduction

While they are commonly treated as three-terminal devices in introductory electronics classes, MOSFETs are actually four-terminal devices. In discrete, three-terminal designs, the body pin and the source pin are tied together internally. In CMOS VLSI design, all four pins play an important role. Having a discrete body pin provides each transistor with its own power or ground reference depending on the type of MOSFET.

In CMOS VLSI design, there are two types of complementary MOSFETs, hence the name CMOS. The two types are the n-channel MOSFET (NMOS) and the p-channel MOSFET (PMOS). N-channel MOSFETs behave like a switch that is normally open, while p-channel MOSFETs behave like a normally closed switch. To change the state of the switch, a voltage $V_{gs}$ is applied to the gate pin.

We will discuss the exact behavior of the two types of MOSFETs further throughout the following two sections. In the final section, we will explore and discuss the properties and behaviors of a CMOS inverter.

### II. NMOS Characteristics

The Shockley first-order model is a good approximation of the relationship between the input voltages and the current through a MOSFET. The model approximates the current through an NMOS $I_{ds}$ is

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \\ \beta\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds} & V_{ds} < V_{dsat} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \end{cases} \quad (1)$$

where $V_{gs}$ is the voltage between the gate and source, $V_t$ is the threshold voltage, $V_{ds}$ is the voltage between the drain and the source, $V_{dsat} = V_{gs} - V_t$, and $\beta$ is a constant based on the physical properties of the MOSFET.

We parametrically varied $V_{gs}$ and $V_{ds}$ using a Python. Then, we plotted $I_{ds}$ using the model described in equation 1. Seen in figure 1, increasing $V_{gs}$ will increase the current. Furthermore, increasing $V_{ds}$ will also increase the current, but only up to a point. After reaching that point, the current does not change with $V_{ds}$.

We then used a simulation tool that takes into account the non-ideal effects of MOSFETs to provide a more accurate plot of the relationship between input voltages and current. First, an NMOS was placed in the schematic, along with some voltage sources with variable voltages. It is important that the voltages be variable, so a parametric test may be run. The final schematic is seen in figure 2.

For the simulation, we set up our output to be the current at the positive terminal of the voltage source V2. We ran a DC sweep simulation of $V_{ds}$, while parametrically stepping through values of $V_{gs}$. The resulting plot is seen in figure 3.

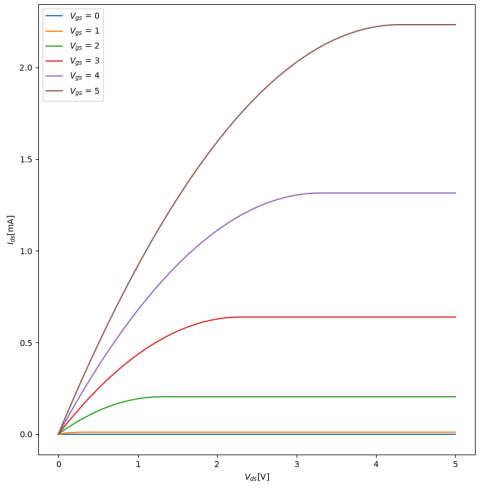


Fig. 1. Plot of Shockley first order model for an n-channel MOSFET

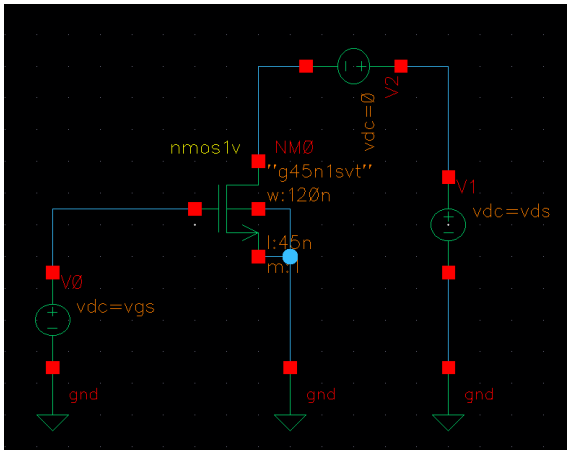


Fig. 2. NMOS parametric test schematic

There is clearly some resemblance between the Shockley model plot and the simulated results. One important difference is that while the curves flatten out completely in the Shockley model, the traces in the simulated NMOS continue to increase well into the saturation region.

### III. PMOS Characteristics

While the source of an NMOS is tied to ground, the source of a PMOS is tied to power.

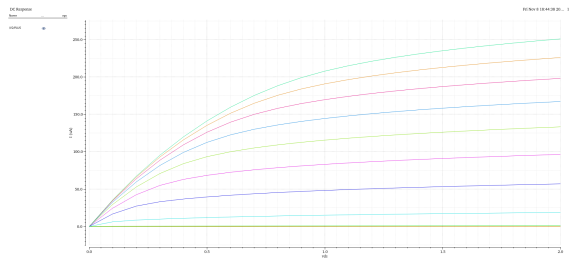

Fig. 3. Simulated relationship between input voltage and NMOS current

**Voltage Naming Conventions—An Aside**

The 'D' in $V_{DD}$ actually stands for "drain" despite connecting to the source of the PMOS. Furthermore, the 'S' in $V_{SS}$ does connect to the source pin of the NMOS. This naming convention dates back to a time when BJT logic was the norm. Specifically, NPN BJT logic. With NPNs, the collector is at the most positive voltage, hence the name $V_{CC}$ corresponding to power. When FET logic became popular, the naming scheme remained the same, but with drains and sources in place of collectors and emitters. Hence, $V_{DD}$ became the name for power, and $V_{SS}$ became the name for ground[1].

PMOS transistors behave the same as NMOS, with the signs of all the voltages and currents flipped[2]. It is also important to note that by changing the signs, the inequalities flip as well, meaning that quantities that must be greater than others for an NMOS are now required to be less, and vice versa. Therefore, the Shockley model for the current through a PMOS is

$$I_{ds} = \begin{cases} 0 & V_{gs} > V_t \\ -\beta\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds} & V_{ds} > V_{dsat} \\ -\frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} < V_{dsat} \end{cases}. \quad (2)$$

With this knowledge, we modified our Python script to model a PMOS. The Shockley model plot seen in figure 4 has the same shape as the plot for the NMOS, but rotated 180° about the origin.

Again, we compared the Shockley model against simulation results. In our schematic, the voltage source for $V_{gs}$ was tied to power instead of ground, and the voltage source for $V_{ds}$ was rotated 180°. Furthermore, the body pin of the PMOS was tied to power instead of ground. All of these changes are seen in the PMOS test schematic seen in figure 5.

Finally, we ran the simulation, this time measuring the current at the drain pin of the PMOS. We swept $V_{ds}$ from -2V to 0V with a step size of 0.1V, and parametrically swept $V_{gs}$ from -2.5V to 0V with a step size of 0.25V. The result was a similar plot to the NMOS simulation, again, rotated 180° about the origin, as seen in figure 6. Another difference between the NMOS and PMOS simulations is the actual values of the current. While the shapes are similar, the PMOS current is less than the NMOS current for the same voltage inputs.

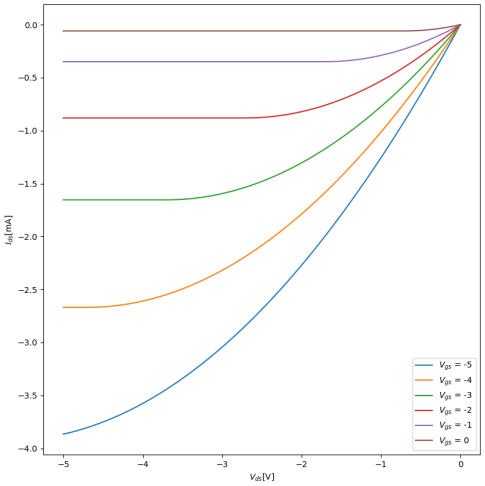


Fig. 4. Plot of Shockley first order model for a p-channel MOSFET

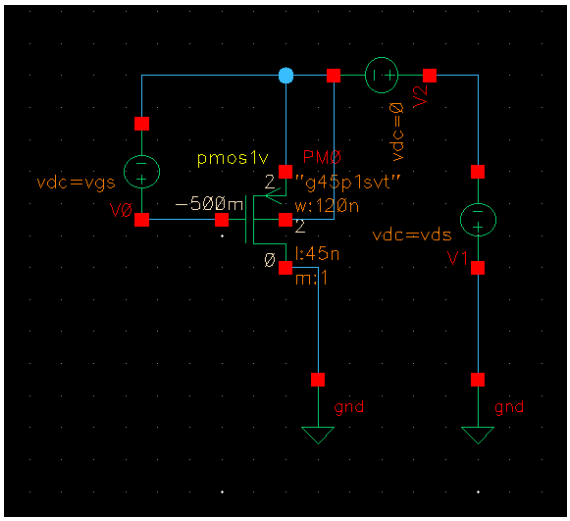


Fig. 5. PMOS parametric test schematic

## IV. The Noise Margin

The noise margin is the amount of noise that a CMOS circuit can withstand without compromising the operation of the circuit[3]. This region is necessary to create a buffer that prevents small amounts of noise from switching the logic. There are two noise margins: noise margin high ($\mathrm{NM_H}$) and noise margin low ($\mathrm{NM_L}$).

The two noise margins are defined in terms of four key voltages on the voltage transfer curve (VTC) seen in figure 7: $V_{\mathrm{IL}}$, $V_{\mathrm{IH}}$, $V_{\mathrm{OL}}$, and $V_{\mathrm{OH}}$. $V_{\mathrm{IL}}$ is defined as the lower input voltage where the slope of the VTC is -1, and $V_{\mathrm{IH}}$ is defined as the upper input voltage meeting the same requirement. $V_{\mathrm{OL}}$ is defined as the output voltage when the input voltage is equal to $V_{\mathrm{IH}}$, and similarly, $V_{\mathrm{OH}}$ is defined as the output voltage when the input voltage is equal to $V_{\mathrm{IL}}$.

Practically speaking, when the input voltage is between $V_{OL}$ and $V_{IL}$ it is interpreted as logic low, and when the input voltage is between $V_{IH}$ and $V_{OH}$ it is interpreted as logic high.

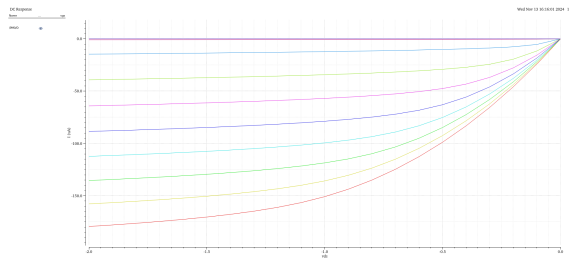

Fig. 6. Simulated relationship between input voltages and PMOS current

The region between $V_{IL}$ and $V_{IH}$ is the "undefined region", where the logic state is unclear [3].

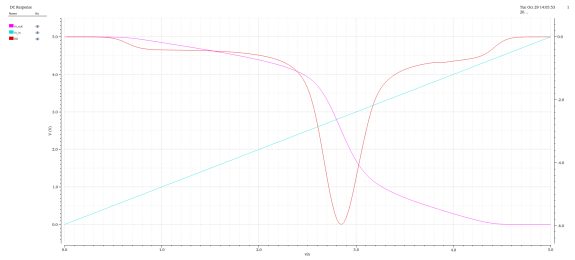

Fig. 7. The VTC and its derivative for a CMOS inverter with $w_p = 240$[nm] and $w_n = 120$[nm]

We pulled the VTC into a calculator tool, and used the definitions for the different voltages associated with the noise margin. Evaluating the expressions produced the values seen in table I.

TABLE I
IMPORTANT VTC VOLTAGES

| | |
|---|---|
| $V_{\mathrm{IL}}$ | 2.357[V] |
| $V_{\mathrm{IH}}$ | 3.531[V] |
| $V_{\mathrm{OL}}$ | 0.683[V] |
| $V_{\mathrm{OH}}$ | 4.118[V] |

With these voltages now defined, the noise margin high was calculated using

$$\mathrm{NM_H} = V_{\mathrm{OH}} - V_{\mathrm{IH}}, \tag{3}$$

and noise margin low was calculated with

$$\mathrm{NM_L} = V_{\mathrm{IL}} - V_{\mathrm{OL}}. \tag{4}$$

Therefore, $\mathrm{NM_H} = 0.587$[V] and $\mathrm{NM_L} = 1.674$[V]. Any voltage existing within the high noise margin would be interpreted as a logic 1 for this inverter, and any voltage existing within the low noise margin would be interpreted as a logic 0. By definition, the larger the noise margin, the more noise the signal can handle without affecting the logic state. Therefore, this inverter can handle more noise when in the logic low state than in the logic high state.

The noise margin is not the same for all inverters, however. To see how the noise margin changes when the MOSFETs used are sized differently, a parametric test was conducted. The width of the NMOS was held constant at 120[nm], but the width of the PMOS was parametrically varied from 120[nm] to 360[nm] with 5 steps in a logarithmic sweep. The resulting VTC is seen in figure 8. This test produced six traces, where the inverter switched at different input voltages, depending on the width of the PMOS.

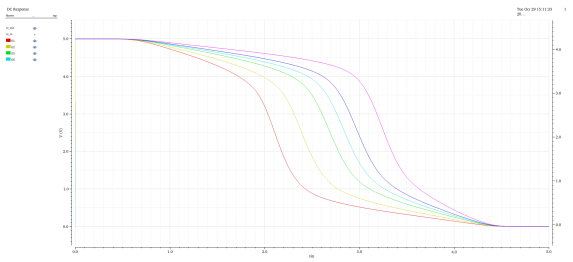

Fig. 8. Inverter VTC for different widths of the PMOS

Again, the VTC was pulled into a calculator tool to determine the derivative, and ultimately, the four voltages associated with the noise margin. Since there were six traces, the result was six derivatives, and a range of values for $V_{OH}$, $V_{IH}$, $V_{OL}$, and $V_{IL}$. The four important voltages were plotted as a function of the width of the PMOS $w_p$, seen in figure 9.

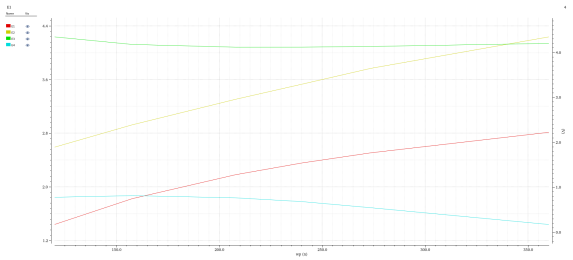

Fig. 9. $V_{OH}$ (green), $V_{IH}$ (yellow), $V_{OL}$ (cyan), and $V_{IL}$ (red) as a function of $w_p$.

Finally, the noise margins were calculated at each $w_p$ using the four already calculated voltages, and the results were plotted in figure 10. The high noise margin shrinks as $w_p$ increases, while the low noise margin grows. However, the sum of $\mathrm{NM_L}$ and $\mathrm{NM_H}$ remains roughly constant, although there is a dip with a minimum where the two noise margins are the same. This means that although the individual noise margins change, the size of the undefined region between logic high and logic low remains about the same. This means that although the individual noise margins change, the size of the undefined region between logic high and logic low remains about the same. This means that although the individual noise margins change, the size of the undefined region between logic high and logic low remains about the same.

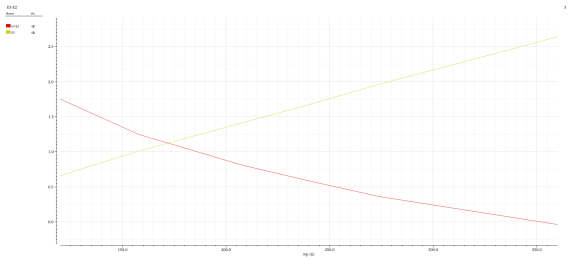

Fig. 10. Resulting $\mathrm{NM_L}$ (yellow) and $\mathrm{NM_H}$ (red).

## V. CONCLUSION

A common theme between analyzing the current through a MOSFET and analyzing the noise margin is the dependence on the physical properties of the MOSFETs.

## References


[1] Olin Lathrop. *What is the difference between VCC, VDD, VEE, VSS*. 2011. URL: https://electronics.stackexchange.com/questions/17382/what-is-the-difference-between-v-cc-v-dd-v-ee-v-ss.

[2] David Money Harris Neil H. E. Weste. *CMOS VLSI Design a Circuits and Systems Perspective, Fourth Edition*. Pearson, 2011.

[3] *Noise Margin*. 2017. URL: https://www.vlsisystemdesign.com/noise-margin/.