VLSI Labs 1&2

Simple MOSFET & CMOS Inverter Trends

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I. Introduction

While they are commonly treated as three-terminal devices in introductory electronics classes, MOSFETs are actually four-terminal devices. In discrete, three-terminal designs, the body pin and the source pin are tied together internally. In CMOS VLSI desin, all four pins play an important role. Having a discrete body pin provides each transistor with its own power or ground reference depending on the type of MOSFET.

In CMOS VLSI design, there are two types of complementary MOSFETs, hence the name CMOS. The two types are the n-channel MOSFET (NMOS) and the p-channel MOSFET (PMOS). N-channel MOSFETs behave like a switch that is normally open, while p-channel MOSFETs behave like a normally closed switch. To change the state of the switch, a voltage V_{gs} is applied to the gate pin.

We will discuss the exact behavior of the two types of MOSFETs further throughout the following two sections. In the final section, we will explore and discuss the properies and behaviors of a CMOS inverter.

II. NMOS Characteristics

The Shockley first-order model is a good approximation of the relationship between the input voltages and the current through a MOSFET. The model approximates the current trhough an NMOS I_{ds} is

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \\ \beta\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds} & V_{ds} < V_{dsat} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \end{cases} \quad (1)$$

where V_{gs} is the voltage between the gate and source, V_t is the threshold voltage, V_{ds} is the voltage between the drain and the source, $V_{dsat} = V_{gs} - V_t$, and β is a constant based on the physical properties of the MOSFET.

We parametrically varied V_{gs} and V_{ds} using a Python. Then, we plotted I_{ds} using the model described in equation 1. Seen in figure 1, increasing V_{gs} will increase the current. Furthermore, increasing V_{ds} will also increase the current, but only up to a point. After reaching that point, the current does not change with V_{ds}.

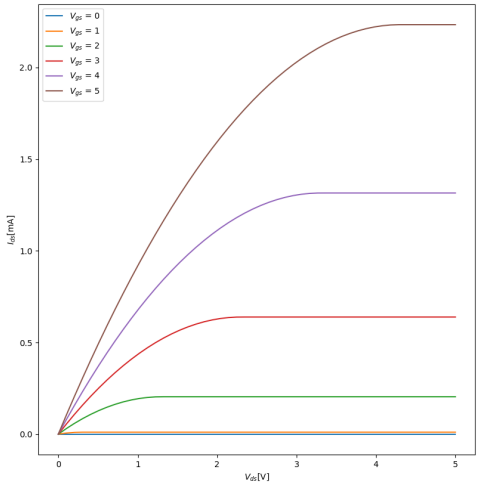

Fig. 1. Plot of Shockley first order model for an n-channel MOSFET

We then used a simulation tool that takes into account the non-ideal effects of MOSFETs to provide a more accurate plot of the relationship between input voltages and current. First, an NMOS was placed in the schematic, along with some voltage sources with variable volages. It is important that the voltages be variable, so a parametric test may be run. The final schematic is seen in figure 2.

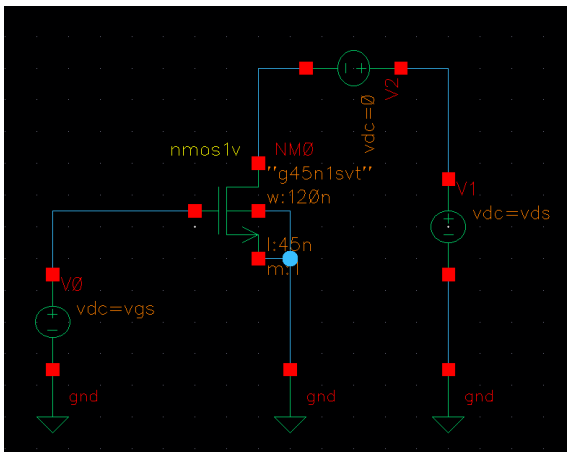

Fig. 2. NMOS parametric test schematic

III. The Noise Margin

The noise margin is the amount of noise that a CMOS circuit can withstand without compromising the operation of the circuit[?]. This region is necessary to create a buffer that prevents small amounts of noise from switching the logic.

There are two noise margins: noise margin high ($\mathrm{NM_H}$) and noise margin low ($\mathrm{NM_L}$).

The two noise margins are defined in terms of four key voltages on the voltage transfer curve (VTC) seen in figure 3: V_{IL}, V_{IH}, V_{OL}, and V_{OH}. V_{IL} is defined as the lower input voltage where the slope of the VTC is -1, and V_{IH} is defined as the upper input voltage meeting the same requirement. V_{OL} is defined as the output voltage when the input voltage is equal to V_{IH}, and similarly, V_{OH} is defined as the output voltage when the input voltage is equal to V_{IL}.

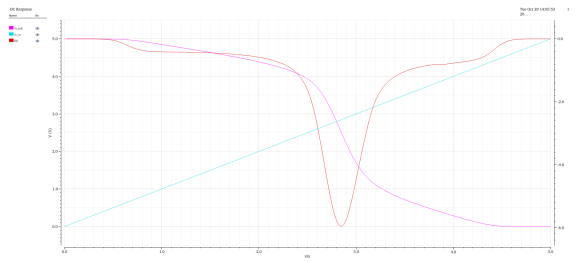

Fig. 3. The VTC and its derivative for a CMOS inverter with $w_p = 240$[nm] and $w_n = 120$[nm]

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TABLE I
IMPORTANT VTC VOLTAGES

V_{IL}	2.357
V_{IH}	3.531
V_{OL}	0.683
V_{OH}	4.118

With these voltages now defined, the noise margin high was calculated using

$$\mathrm{NM_H} = V_{\mathrm{OH}} - V_{\mathrm{IH}}, \tag{2}$$

and noise margin low was calculated with

$$\mathrm{NM_L} = V_{\mathrm{IL}} - V_{\mathrm{OL}}. \tag{3}$$

IV. Discussion

V. Conclusion