CMOS VLSI Design

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Contents

Chapter 1

CMOS Circuits, Fabrication, and Layout Design Rules

1.1 A Brief History

First transistor developed at Bell Labs in 1947.

1.2 MOSFET Overview

MOSFETs are four-pin devices (source, gate, drain, body). The gate and body are conductors, while the source and drain are semiconductors. For nMOS devices, the body pin should always be tied to the lowest potential. For a pMOS device, the body pin is tied to the highest potential.

> **Note:**
> For CMOS circuits, the output power always comes from the rails, not the gate.

1.2.1 Power Supply Voltage

- GND = 0V

- In 1980's V_{DD} = 5V

- V_{DD} has decreased over time

- 3.3V and 1.2V CMOS circuits are common today

1.3 CMOS Transistor Theory

A transistor that is on passes a finite amount of current dependent on terminal voltages. The gate, source, and drain all have capacitance. Capacitance and current determines the speed and timing of these devices.

$$I = C\frac{dv}{dt} \tag{1.1}$$

MOSFETs have operation modes: accumulation, depletion, and inversion. These modes depend on the voltages V_g, V_d, and V_s. Source and drain are symmetric diffusion terminals, but by convention, the source is the terminal at lower voltage; hence, $V_{ds} \geq 0$. The body of an nMOS should be grounded, and, at this point, it is safe to assume that the source terminal is also grounded.

MOSFETs also have regions of operation: cutoff, linear, and saturation. During cutoff, $I_{ds} \approx 0$. During the linear region, $I_{ds} \propto V_{gs}$, and during the saturation regions, increasing voltage no longer increases current.
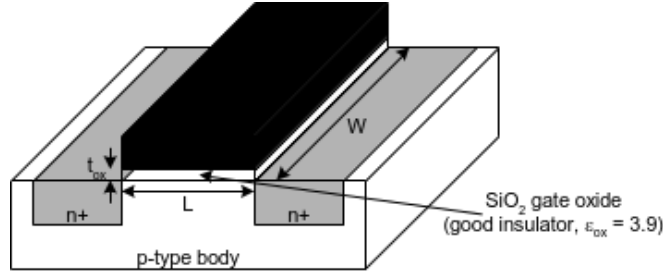
$$Q_{\text{channel}} = CV \tag{1.2}$$

Figure 1.1: nMOS dimensions

$$C = C_g = \varepsilon_{\text{oxide}} \frac{WL}{t_{\text{oxide}}} = C_{\text{oxide}} WL \tag{1.3}$$

$$C_{\text{oxide}} = \frac{\varepsilon_{\text{oxide}}}{t_{\text{oxide}}} \tag{1.4}$$

Electrons are propelled by the lateral electric field between source and drain $E = V_{ds}/L$.

If $V_{gd} < V_t$, the channel pinches off near the drain, meaning that an increase in voltage does not cause an increase in current.

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \\ \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & V_{ds} < V_{\text{saturation}} \\ \frac{\beta}{2} \left(V_{gs} - V_t \right)^2 & V_{ds} > V_{\text{saturation}} \end{cases} \tag{1.5}$$

Since pMOS transistors pass power rather than creating a ground connection, they must be larger than nMOS transistors. For the case of this class: $\mu_p = 2\mu_n$.

1.4 Capacitance

The gate capacitance per micron is typically about 2fF.

1.5 Logical Gate Truth Tables

Table 1.1: Truth table of a NOT gate

in	out
1	0
0	1

Table 1.2: Truth table of a NAND gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

With the goal to set the correct output to V_{DD} and GND, shorts must be avoided. Simple guides:

1. nMOS can only pass "0"

2. pMOS can only pass "1"

3. Always use pMOS in a pull-up network and nMOS in a pull-down network, with the output between them

4. Only one of the two networks should be on at any given time

1.5.1   Implementing Arbitrary Functions

Realize the pull-down network by inspection (looking at the truth table), and then use deMorgan's theorem to manipulate.

Example 1.5.1

Given the function $F = \overline{A + BC}$, the pull-down network implements A OR B AND C. Keep in mind that MOSFETs in series have the effect of AND, and MOSFETs in parallel have the effect of OR. Next, use deMorgan's theorem to implement $\overline{A + BC}$ as a non-inverted function. This becomes $\bar{A} \cdot (\bar{B} + \bar{C})$. Finally, combine the pull-up and pull down networks.

1.6   Nonideal Transistor Theory