Lab 1: I-V Family of Curves

a) Log into Cadence

Each time you log in you will need to do the following:

i) source cds.setup

ii) cd cadence

iii) virtuoso &

b) The Library Manager

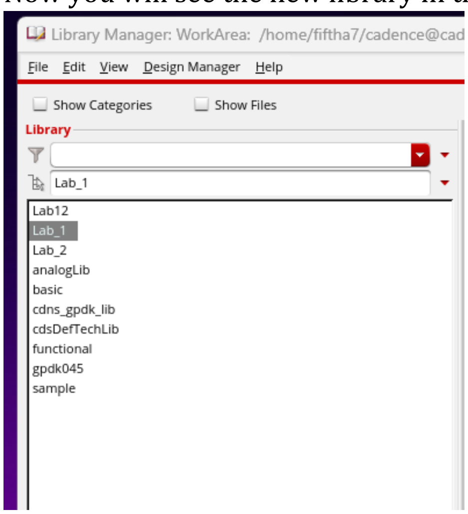
From the **Library Manager**: create a new library with a name **Lab_1:**

i) Choose File -> New -> Library, then put your library name, **Lab_1** and click **OK**.

ii) Choose **Attach to an existing technology library** (3rd option down)

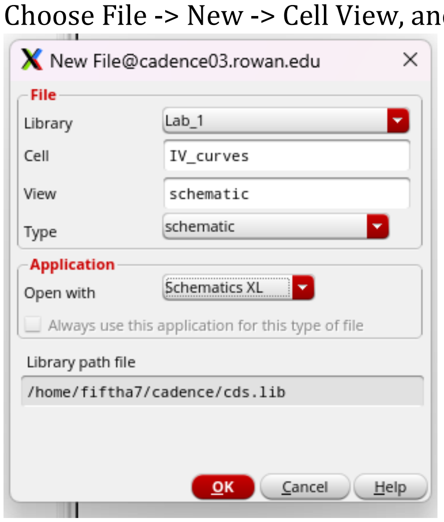
iii) Select **gpdk045**, then **OK**.

iv) Now you will see the new library in the Library Manager.



Then from the **Library Manager**: create a new cell, named **IVcurves**

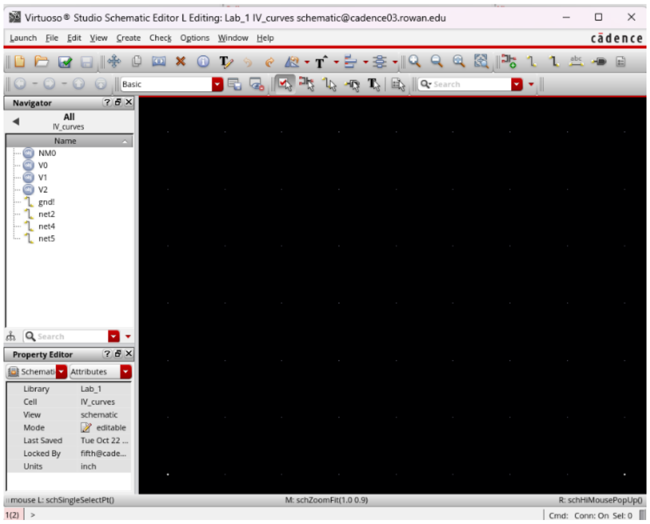
v) Choose File -> New -> Cell View, and select **Lab_1** as the library name



vi) Type **IVcurves** in Cell, and **schematic** in View

vii) Choose **Schematics XL** for the Application/Open with, and check for the checkbox

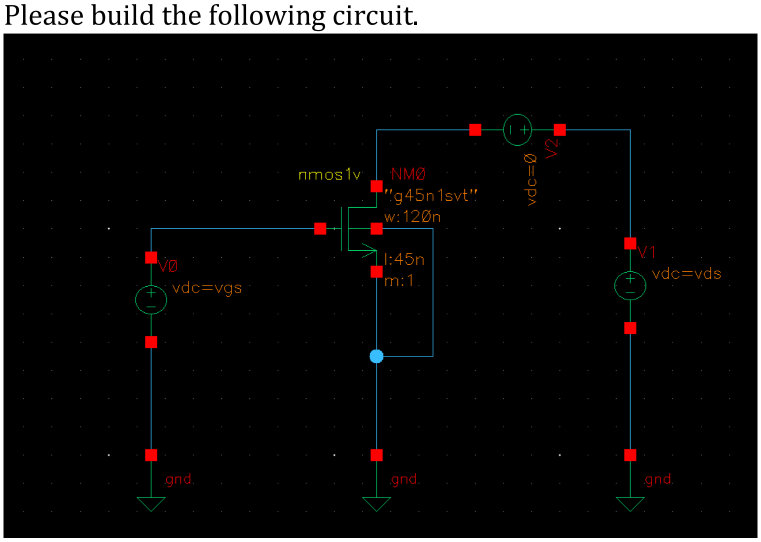
viii) Clicking **OK** will **open Virtuoso Schematic Editor XL** with an empty black panel. As shown below.



c) Build Your Circuit

i) Selecting create -> Instance opens the component browser where parts can be chosen for your schematic.

ii) Please build the following circuit.



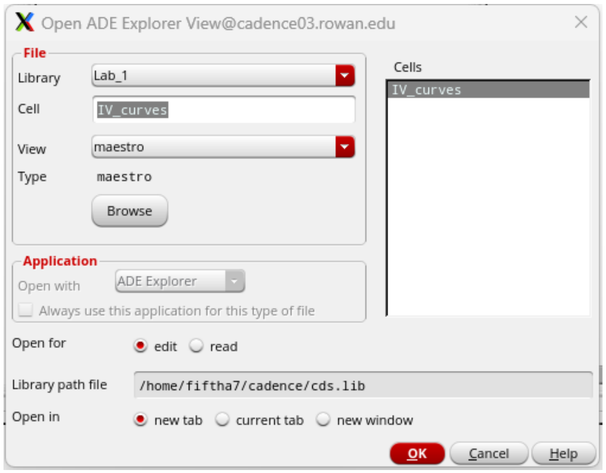
The NMOS, **nmos1v**, can be selected via the content browser under **gpdk045**.
(I have not tested out any of the other NMOS spice files yet, you are more than welcome to test those out and report back to me if or how well they work.)
The voltage source, **vdc**, and ground, **gnd,** can be found under **analogLib.** Wire up the circuit by selecting the **Create Narrow Wire** tool on the **Quick Edit ribbon**.

iii) We are going to use this circuit to perform a parametric sweep and plot out the family of curves for this transistor. Therefore, we are going to have to use variables for the sources we want to change.
Set the gate and source voltages to a parameter **vgs** and to **vds**, respectively. (The **properties** can also be changed by selecting an instance and **pressing Q** or right clicking and selecting properties.)

iv) **SAVE YOUR WORK!!!**

d) Test Your Circuit

i) In the Schematic Editor, go to Toolbar-> Launch ADE Explorer -> Create new view.



ii) Select your cell design and correct library name in ADE Explorer

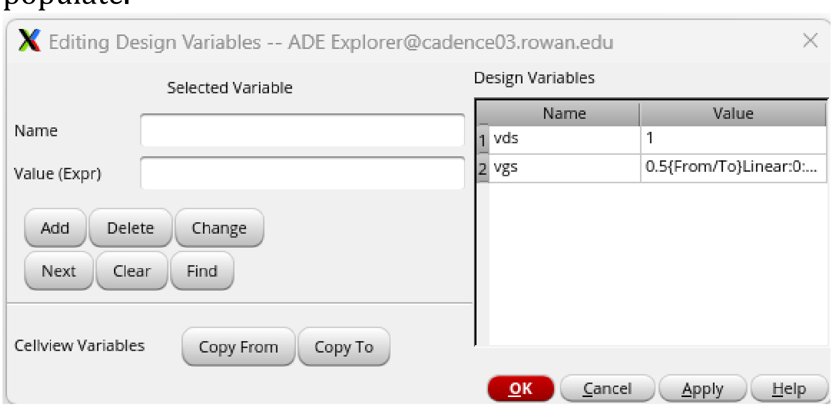
iii) To Change your simulation tool: In the test editor window, select the drop-down Setup -> Simulator and change the simulator to spectre (it should already be selected)

i) Then add the model libraries by selecting the drop-down Setup -> Model Libraries in the test editor window and add the following path to the list: /home/cadencelibs/gpdk045_v_6_0/gpdk045/../models/spectre/gpdk045.scs

ii) On the right side of the Model File path you will see a section column, click on that and change it from mc ->tt and save.

iii) From here you can use the top toolbar or the setup menu on the left hand side of your screen to set up you test. I find it easier to use the left panel.

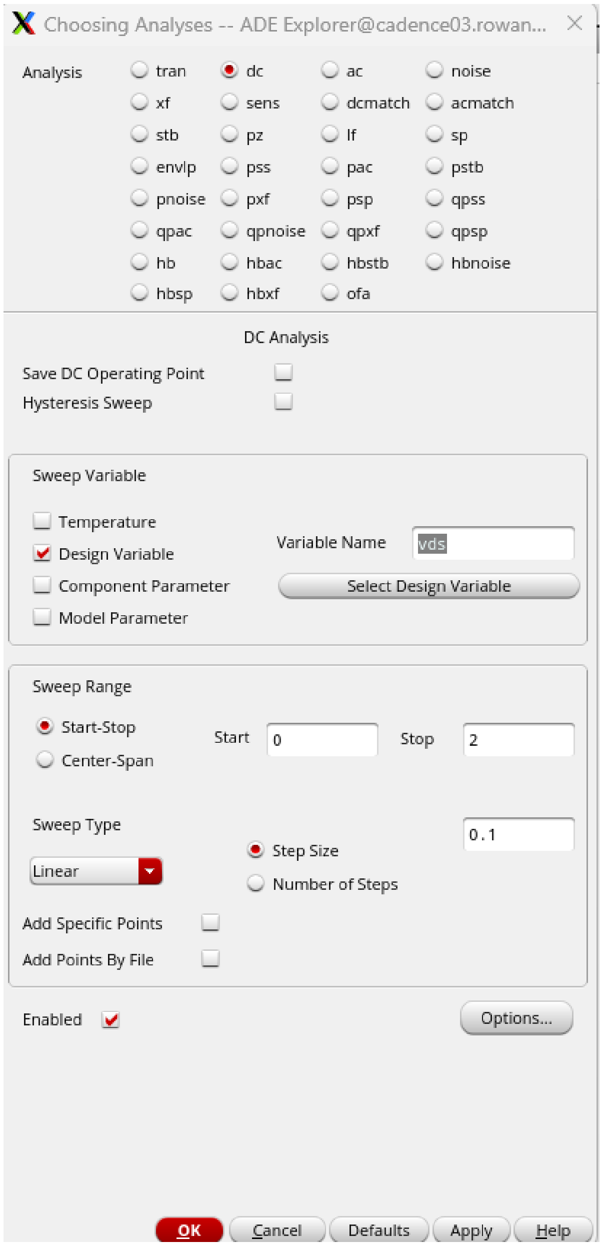
iv) Under Design variables you will see grayed out text "Click to add veriable", click on that and select "Copy From" and you will see you schematic veriables populate.



Initially you will have no values assigned to those variables, choose an appropriate initial value for those variables. (I chose vgs=0.5 and vds=1.)

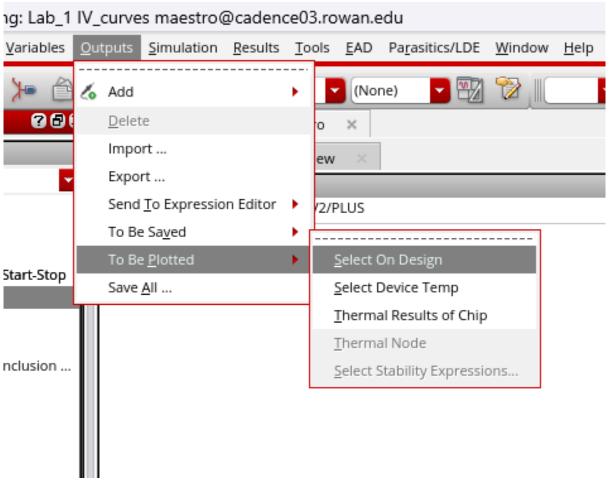
v) Then define your analysis follow the same method you did for design variables. Under **Analyses** select "Click to add analysis".

vi) Make sure you have the correct options selected on the Analysis window to get the test to work. The values are in the window below:

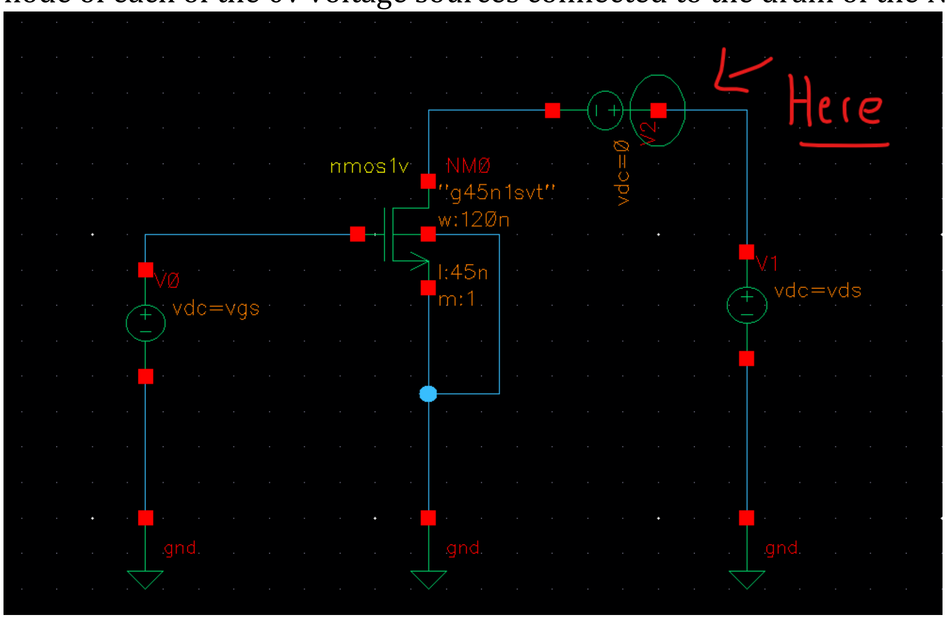


Under **Analyses** add a **dc analysis** with the design variable set to **vds**, with the start-stop range from 0 to 2.5 in linear steps of 0.1.

vii) Now define the outputs to be plotted. This is done through the top menu bar.

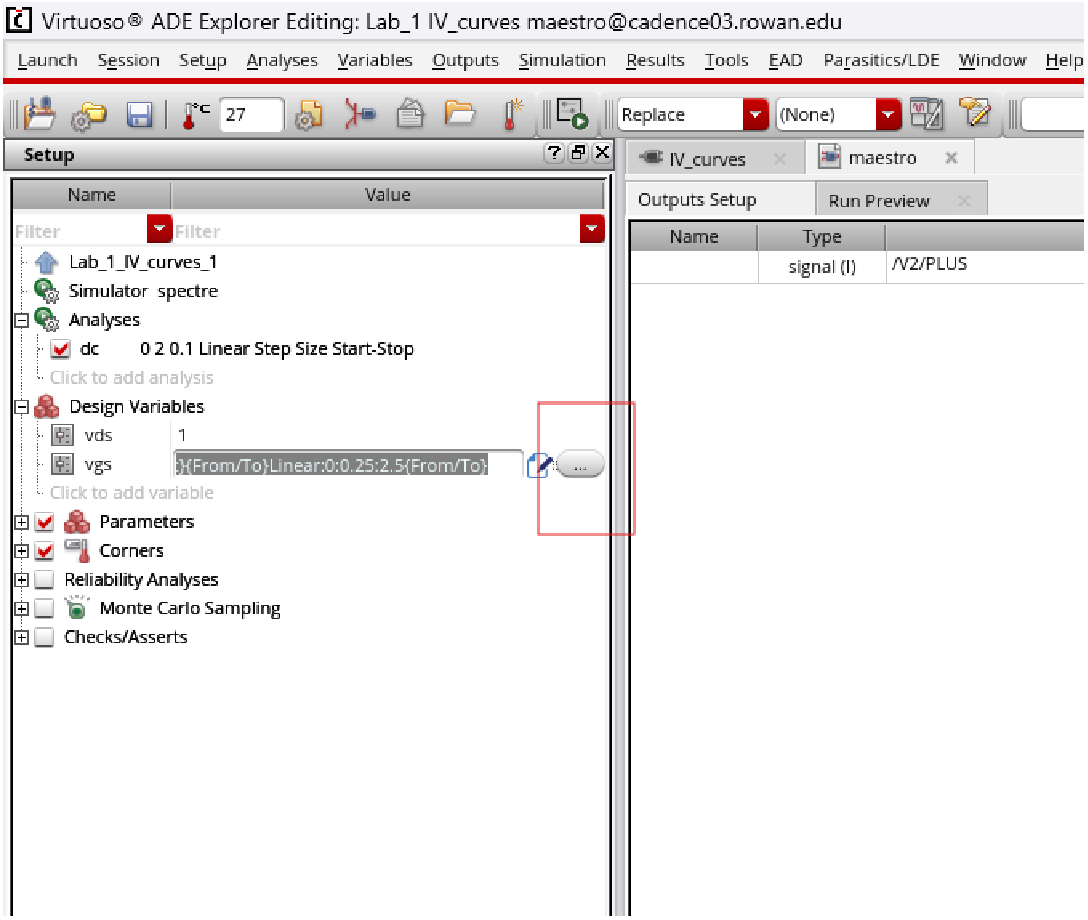


Outputs -> To be plotted -> select on design. (You can also type them in if you choose but keep in mind Cadence is case sensitive.) We want to measure the current on the drain of the NMOS with varying vgs. Please select the positive node of each of the 0v voltage sources connected to the drain of the NMOS.

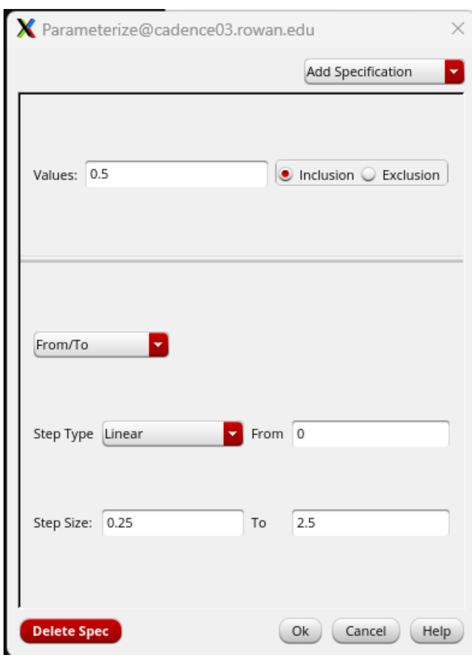


viii) Add the parametric sweep:

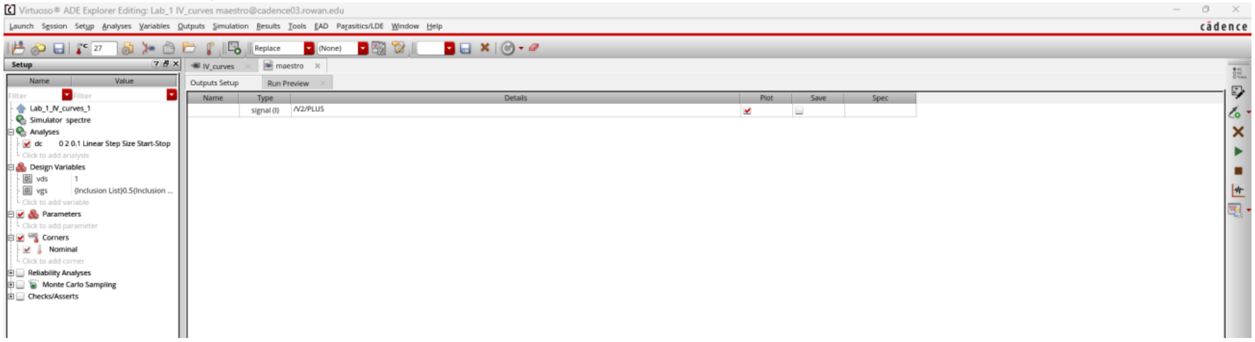
(1) Click on the 3 dots next to the variable you want to iterate (vgs for this lab)



Use these values:



ix) This should be your setup:



x) Save and hit the green play button to run the simulation.

xi) The results should look something like this:

b) PMOS IV-Curves

i) On your own, please re-work the circuit using a PMOS and repeat the parametric analysis. You may need to refer to your Electronics textbook for the schematic setup.

ii) Create a new cellview in the same library. Pick proper sweep ranges for vds and vgs. Plot Id vs Vsg.