VLSI Exam 1 Section 1 - Aidan Sharpe

Problem 1

Aluminum is a suitable material when access to polysilicon is restricted. Restrictions may be in terms of access or the cost of the material. Academic institutions, for example, would not have access to polysilicon.

Problem 2

```
L_n = 0.6E-6
L_p = 0.6E-6

K_n = 122E-6
K_p = 61E-6

C_ox = 33E-4

V_tn = 0.7
V_tp = -0.7

V_gs = 5
V_ds = 5

V_dsat = V_gs - V_tn

I_ds = 2.82E-3
```

2a

```
w_n = (2*I_ds*L_n) / (K_n * V_dsat**2)
```

$W_n = 1.5[\mu\text{m}]$

2b

```
w_p = (2*I_ds*L_p) / (K_p * V_dsat**2)
```

$W_p = 3[\mu\text{m}]$

2c

Inverter input capacitance: 3C

Fanout capacitance 9C

Total load capacitance: 12C + 22μF

```
C_g = C_ox*w_n*L_n
C_equiv = 12*C_g + 20E-15
```

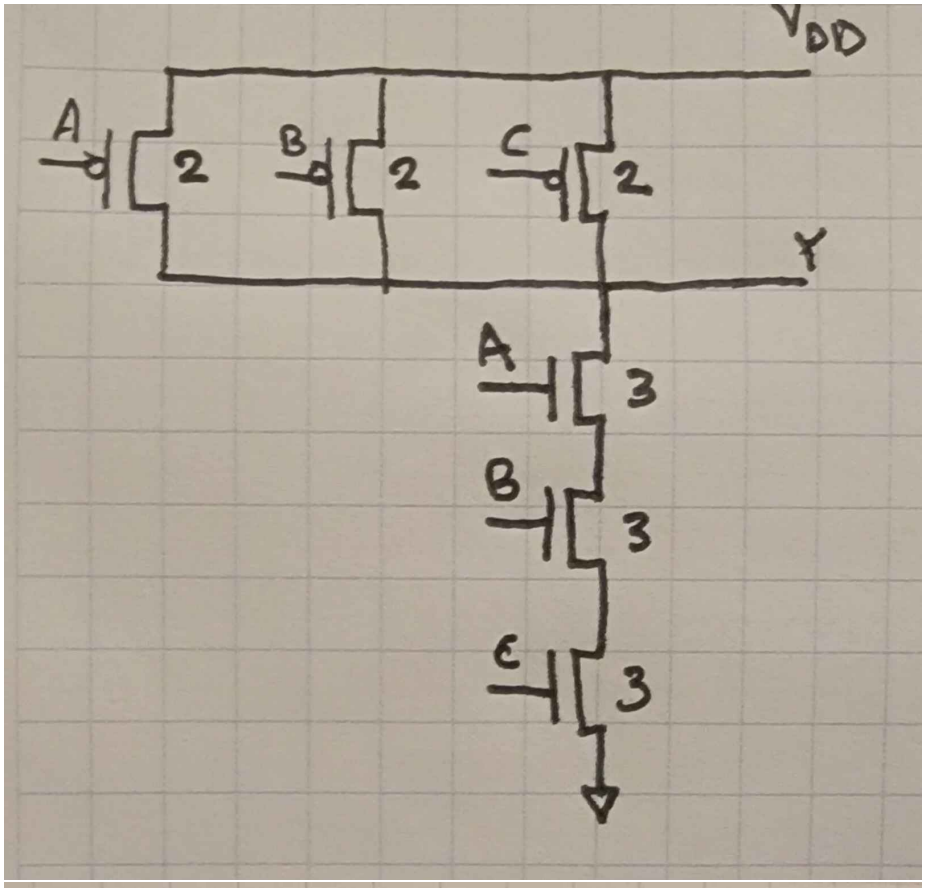
```
beta = K_n*w_n/L_n
I_sat = beta * (V_gs - V_tn)**2 / 2
t_sat = V_tn*C_equiv / I_sat
R = 10E3
tau = R*C_equiv
t_lin = -tau*log(0.5/4.3)
t = t_lin + t_sat
```

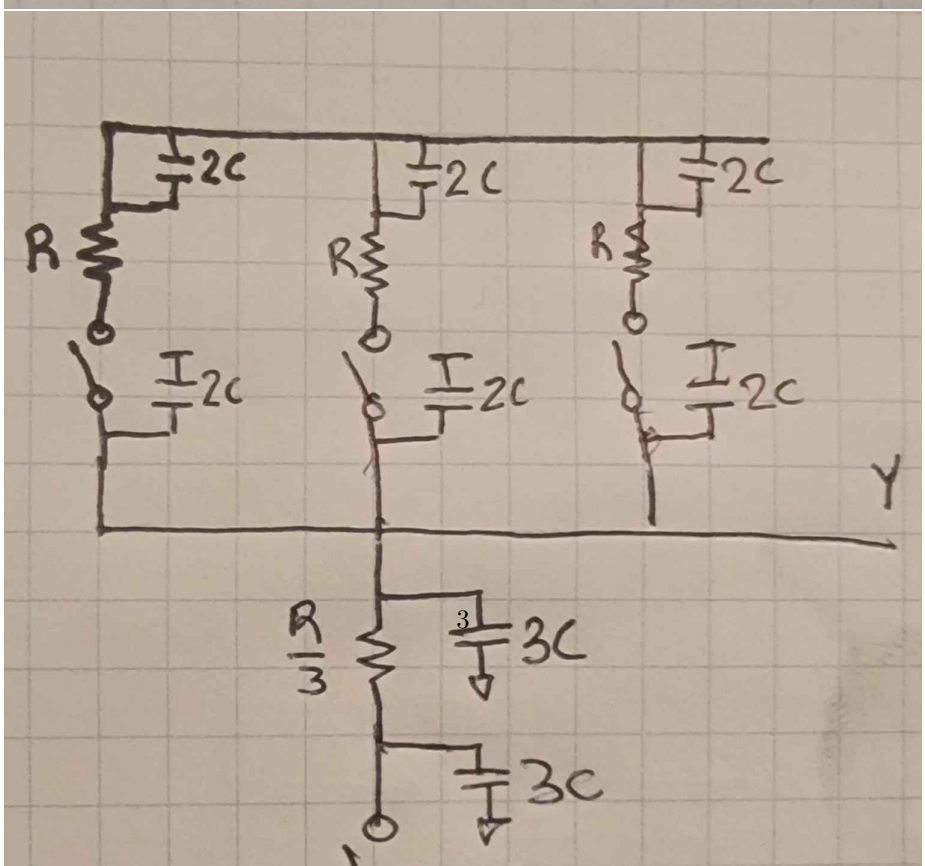
$t_{\text{sat}} = 13.81[\text{ps}]$

$t_{\text{lin}} = 1.19[\text{ns}]$

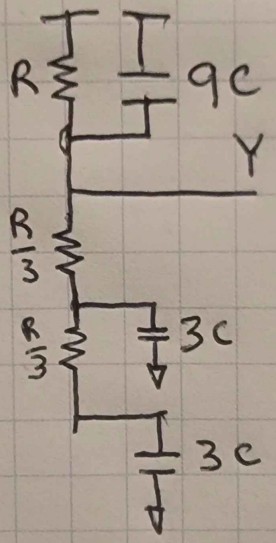
$t = 1.21[\text{ns}]$

2d

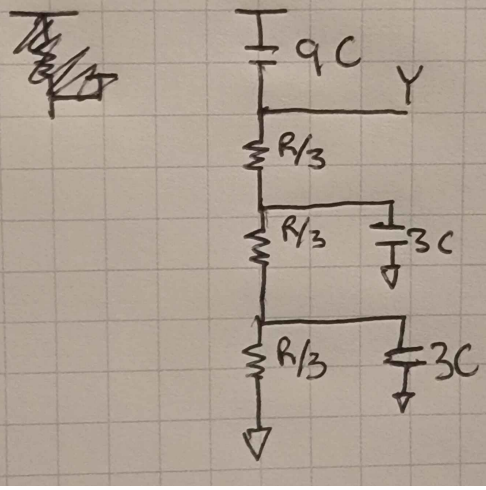




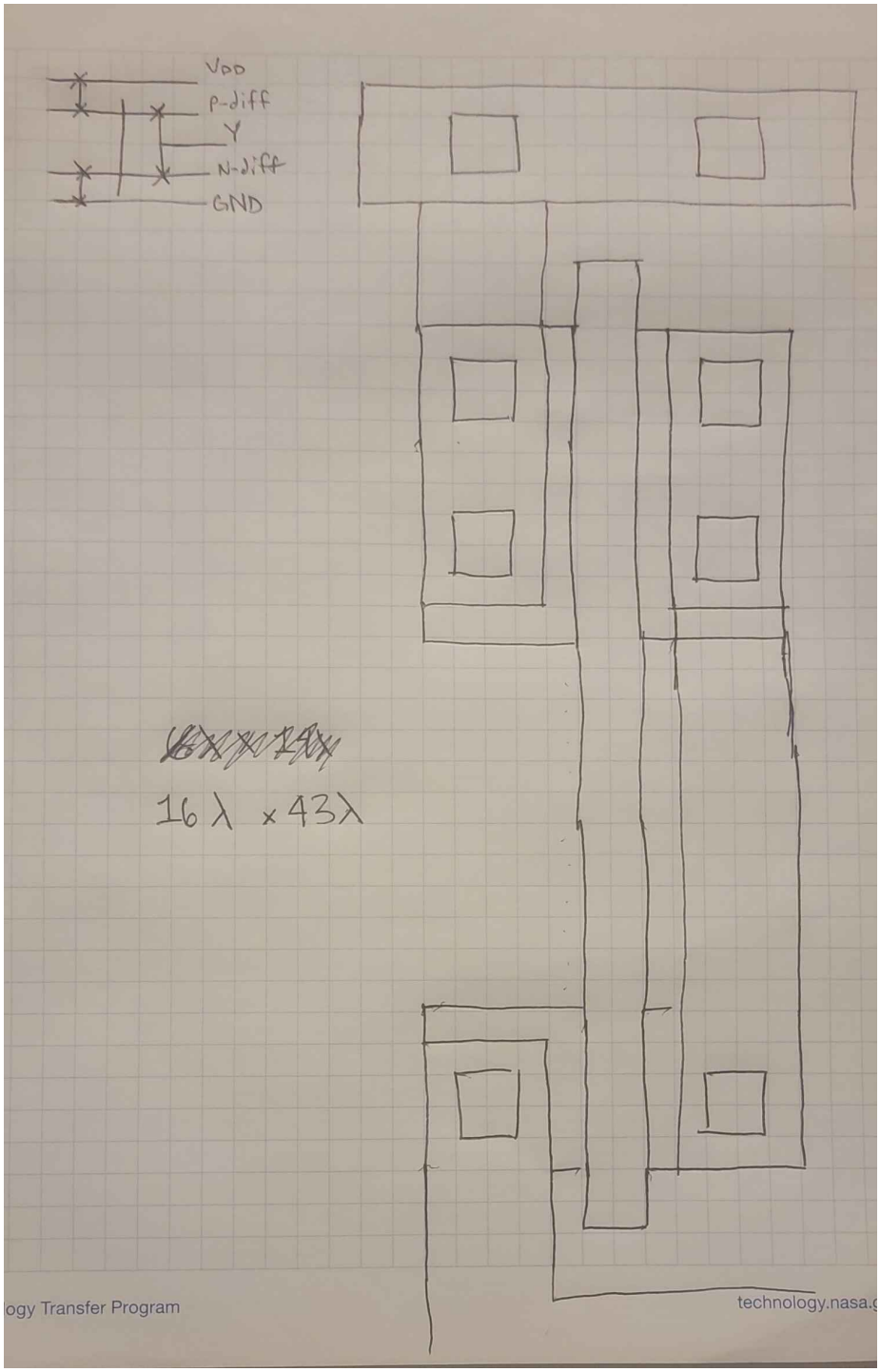
Pull-Up Network (RC & Elmore)



Pull-Down Network (RC & Elmore)



2e



Since there is only one capacitor node, the Elmore delay and the RC delay are

the same.

For both:

`t_pd = R*C_equiv`

$t_{pd} = 556.43$[ps]