VERY LARGE SCALE INTEGRATION (VLSI) DESIGN
ECE 09.414
FALL 2024

Instructor: Prof. Adam Fifth
Office Location: Engineering Hall (ENGR 332)
E-mail: Canvas only please

Lab Instructor: TBD

Class Meeting: Section 1: TR 0800-0915 ENGR 338
Section 2: TR 1530-1645 ROWAN 117

Lab Hours: Section 1: T 0930-1215 ENGR 338
Section 2: F 1100-1345 ENGR 320

Office Hours: TBD

Prerequisites: ECE 09.311 Electronics I

Reference Texts: CMOS VLSI Design: A Circuits and Systems Perspective, 4th edition.
ISBN-13: 9780137981076

Academic Calander:
Labor Day (no classes) Monday, September 2
Semester Classes Begin Tuesday, September 3
Thanksgiving Recess (no classes) Thursday-Saturday, November 28-30
Reading & Review (no classes) Thursday, December 12
Finals Week Friday-Thursday, December 13-19 (includes Saturday, December 14)
Flexible Time Day Friday, December 20

Safety First

This class has a lab component that is simulation based but you will occasionally be in the lab rooms with the electronic equipment. Therefore, you are required to complete the ECE Safety Training by visiting https://go.rowan.edu/ecerc. After signing in select Safety Training. Upon completing viewing the safety videos, you must take and pass the test, which will then give you a certificate that is good for one year. Submitting your certificate is Assignment 0. If you do not submit that certificate, you will not be allowed in the lab, which will inevitably lead to a failing grade.

ABOUT THIS CLASS & OBJECTIVES

The course focuses on team-oriented design projects to demonstrate the impact of circuit family choice and microelectronic processing on circuit design. The course will cover basic theory and

techniques of digital VLSI design in CMOS technology. Topics include CMOS devices and circuits, fabrication processes, static and dynamic logic structures, chip layout and layout design rules, simulation and testing, memories and array structures. We use full-custom techniques to design basic logic gates. Students will design a project test circuit using various Cadence CAD tools. Circuits will be verified and analyzed for performance with various simulators and the impact of process choice will be demonstrated. **(3 credits)**

NOTE: This course consists of a lecture and a laboratory component. The lab component has an oral presentation component. The oral presentation must be completed as part of the course outcome and cannot be substituted. The presentation is conducted in the last 3 weeks of the semester including finals week so there is plenty of time to complete the presentation for almost any situation.

COURSE OUTCOMES & PERFORMANCE INDICATORS

This course is intended to provide the student with the basic capability to design, analyze, characterize, and optimize transistor level circuits. Current VLSI issues such as noise analysis, power delivery, power management, timing analysis, floor-planning/integration, and transistor/wire scaling will be covered.

Students participate in a design process that incorporates realistic engineering constraints such as manufacturability and economics, as well as issues dealing with safety and ethics.
Upon successful completion of this class, you will be able to understand the modern CMOS technology, use the state-of-the-art VLSI design suite (Cadence) for a broad spectrum of VLSI applications.

The following general performance indicators will be used to assess whether you and this class have met the course objectives and outcomes.

- Use mathematical methods and circuit analysis models in analysis of CMOS digital electronic circuits, including logic components and interconnects.
- Create models of moderately sized CMOS circuits that realize specified digital functions.
- Understand the concepts of power and delay in digital circuits.
- Apply logical efforts method to design digital chips and analyze VLSI circuit timing.
- Design digital logic circuits and draw layout diagram.
- Use Cadence in the design and simulation of digital circuits.
- Analyze and interpret data produced by Cadence.
- Understand concepts of CMOS design rules, trends in semiconductor technology, and how it impacts scaling and performance.
- Apply CMOS technology-specific layout rules in the placement and routing of transistors and interconnect, and to verify the functionality, timing, power, and parasitic effects.

- Complete a significant VLSI design project having a set of objective criteria and design constraints.
- Plan, execute and optimize an individual design project.
- Identify the characteristics of various CMOS circuit construction, and to compare between different state-of-the-art CMOS technologies and processes for solving engineering problems.
- Design VLSI system for given constraints.
- Disseminate outcomes of their design in appropriate formats for technical communications.
- Effectively present their experiments and design to the class.
- Utilize Matlab to characterize transistor behaviors, power and delay of VLSI circuits, and to optimize circuit parameters for given constraints.

ABET CRITERIA (STUDENT OUTCOMES) MET BY THIS COURSE

The outcomes of this course – assessed by a combination of in class quizzes, homework, midterm and final exams, weekly laboratory design exercises, final design project, as well as attendance and professionalism – meet the following ABET criteria.

Outcome 1: An ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics.

1.1 Application of Math Models and Circuit Analysis: Students will be able to use mathematical methods and circuit analysis models in analysis of CMOS digital electronics circuits, including logic components and their interconnects.

1.2 Developing CMOS Models: Students will be able to create models of moderately sizes CMOS circuits that realize specified digital functions.

1.3 VLSI System Design: Students will be able to design VLSI systems for given constraints.

Outcome 3: An ability to communicate effectively with a range of audiences.

3.1 Technical Writing: Students will be able to disseminate outcomes of their designs in appropriate formats for technical communications.

3.2 Technical Presentation: Students will be able to effectively present their experiments and design to the class.

Outcome 6: An ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgement to draw conclusions.

6.1 Applying and Verifying CMOS Layouts: Students will be able to apply CMOS technology-specific layout rules in the placement and routing of transistors and interconnect, and verify the functionality, timing, power, and parasitic effects.

6.2 Characterize and Analyze Realistic Behaviors: Students will be able to utilize engineering tools to characterize and analyze transistor behaviors, power and delay of VLSI circuits, and to optimize circuit parameters for given constraints.

6.3 Design Based on Given Objective and Constraints: Students will be able to complete a VLSI design project given a set of objective criteria and design constraints.

6.4 Engineering Design Project: Students will be able to plan, execute, and optimize an engineering design project.

Outcome 7: An ability to acquire and apply new knowledge as needed, using appropriate learning strategies.

7.1 CMOS Design Rule Concepts: Students will be able to understand concepts of CMOS design rules, trends in semiconductor technology, and how it impacts scaling and performance. parasitic effects.

7.2 Cadence Design: Students will be able to use Cadence in the design and simulation of digital circuits.

7.3 CMOS Design Comparisons: Students will be able to identify the characteristics of various CMOS circuit construction, and to compare between different state-of-the-art CMOS technologies and processes for solving engineering problems.

7.4 Transistor Characterization: Students will be able to utilize computer-based tools to characterize transistor behaviors, power and delay of VLSI circuits, and to optimize circuit parameters for given constraints.

COURSE PREREQUISITES

This course builds upon concepts that you have learned in ECE 09.342 Introduction to Embedded Systems. It is your responsibility to come to class equipped with the knowledge and background provided in those courses. The following is a brief list of topics that are of utmost importance and hence need your particular attention before you come to this class.

- *Basic knowledge of semiconductor physics, MOSFET characteristics, and circuit theory*
- *Basic concepts of digital logic elements and working knowledge of CMOS logic design*

COURSE OUTLINE:

1. **CMOS: Circuits (Chapter 1)**
    - Brief History
    - Course Summary
    - MOS Transistors – Simplified view
    - CMOS Logic
2. **MOS Transistor Theory (Chapter 2)**
    - Basic Semiconductor Physics
    - Ideal I-V characteristics
    - C-V Characteristics
    - Non ideal I-V Effects
    - DC Transfer Characteristics
    - Gate and Diffusion Capacitances
3. **Delay - DC and Transient Response (Chapter 4)**
    a. DC Response
    b. Logic Levels and Noise Margin
    c. Transient Response
    d. Delay Estimation
    e. Logical Effort and Transistor Sizing

Examination # 1

4. **Fabrication and Layout Rules (Chapter 1 & 3)**

- CMOS Fabrication
- Layout Design Rules
- Design Partitioning
- Example: A Simple MIPS Processor
- Logic Design
- Circuit Design
- Physical Design
- Design Verification
- Fabrication, Packaging and Testing

5. **Power (Chapter 5)**
    - Power and Energy
    - Static Power
    - Dynamic Power
6. **Interconnect (Chapter 6)**
    - Introduction
    - Interconnect Modeling
    - Wire RC Delay
    - Crosstalk
    - Wire engineering
    - Repeaters
7. **Robustness and Transistor Scaling (Chapter 7)**
    - Variation
    - Noise Budget
    - Reliability
    - Circuit Pitfalls
    - Transistor Scaling
8. **Circuit Simulation (Chapter 8)**
    - Introduction to SPICE
    - DC Analysis
    - Transient Analysis
    - Sub circuits
    - Optimization
    - Power Measurement
    - Logical Effort Characterization

Examination # 2

9. **CMOS Logic and Circuit Design (chapter 9)**
    - Combinational Circuit Design
    - Circuit Families
    - More Circuit Families
    - Comparison of Circuit Families
10. **Array Subsystems - Memories and Array Structures (Chapter 12)**
    - Introduction
    - SRAM
    - DRAM
    - ROM

- Serial Access Memories
- Content-Addressable Memory
- Programmable Logic Arrays
- Array Yield, Reliability and Self-test

Presentations

GRADING SCALE

There will be two mid-term exams and a comprehensive final exam. An absolute / curved grading scheme will be used to assess your final grade.

Category weightings are as follows:

Homework	10 %
Attendance	0 %
Quiz	10 %
Labs	15 %
Midterm Exams (x2)	40 %
Final	25%
Total	100%

Homework: Homework is due according to the schedule laid out on Canvas and solutions will be posted the morning after it is due. Once the solutions are posted any outstanding homework will be given a zero. Homework's will be graded as complete/incomplete (i.e. all or nothing) and will not be graded on accuracy. For a "complete" you will need to attempt each part of every problem ("I don't know" is not considered an attempt to complete the problem).

Attendance: I take attendance for the benefit of the student. Missing classes will greatly reduce your understanding of the material and result in lower grades.

Quizzes: There will be 8-12 quizzes over the course of the semester. No matter how many quizzes I give I will always drop the lowest 2. For this reason, I do not give makeup quizzes. If you miss a quiz that one will be counted as a 0 and removed at the end of the semester.

Exams: There are 2 exams over the course of the semester but no final. The project will take the place of the final exam.

ACCOMMODATION FOR DISABILITY & ACADEMIC SUCCESS CENTER

Your academic success is important. If you have a documented physical and/or learning disability, please inform the Academic Success Center (ACS; director: John Woodruff – woodruff@rowan.edu, or 256-4234) regarding what kind of accommodation you need to help you succeed in this class. While you are not required to disclose details of your disability to me, you must provide appropriate documentation to the ACS to receive official university assistance. I can only provide special accommodation if I receive a letter describing the nature of such accommodation from the ACS. Accommodation requests without a letter from ACS cannot be honored. All such

requests will be held confidential to the extent possible. Please visit the following page for additional details and instructions: http://www.rowan.edu/studentaffairs/asc/disabilityresources/ .

Academic success center also provides a variety of other services, including tutoring services, which are all typically free. I encourage you to take advantage of these services. Please contact them at 304 Savitz Hall, or by visiting their website at http://www.rowan.edu/studentaffairs/asc/

You may also be interested in the Rowan Success Network, designed to make it easier for you to connect with the resources you need to be successful at Rowan. Throughout the term, you may receive email from the Rowan Success Network team (Starfish®) regarding your academic performance. Please pay attention to these email and consider taking the recommended actions. Utilize the scheduling tools to make appointments at your convenience including tutoring. Additional information about RSN may be found at www.rowan.edu/rsn.