VLSI Labs 1&2

Simple MOSFET & CMOS Inverter Trends

Aidan Sharpe

I. Introduction

II. Modelling a MOSFET

III. The Noise Margin

The noise margin is the amount of noise that a CMOS circuit can withstand without compromising the operation of the circuit[**?**]. This region is necessary to create a buffer that prevents small amounts of noise from switching the logic. There are two noise margins: noise margin high ($\mathrm{NM_H}$) and noise margin low ($\mathrm{NM_L}$).

The two noise margins are defined in terms of four key voltages on the voltage transfer curve (VTC) seen in figure 1: V_{IL}, V_{IH}, V_{OL}, and V_{OH}. V_{IL} is defined as the lower input voltage where the slope of the VTC is -1, and V_{IH} is defined as the upper input voltage meeting the same requirement. V_{OL} is defined as the output voltage when the input voltage is equal to V_{IH}, and similarly, V_{OH} is defined as the output voltage when the input voltage is equal to V_{IL}.

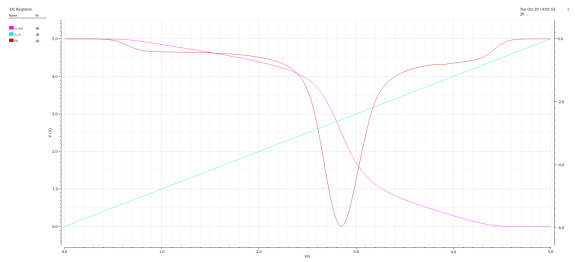

Fig. 1. The VTC and its derivative for a CMOS inverter with $w_p = 240$[nm] and $w_n = 120$[nm]

.

TABLE I
Important VTC voltages

V_{IL}	2.357
V_{IH}	3.531
V_{OL}	0.683
V_{OH}	4.118

With these voltages now defined, the noise margin high was calculated using

$$\mathrm{NM_H} = V_{\mathrm{OH}} - V_{\mathrm{IH}}, \tag{1}$$

and noise margin low was calculated with

$$\mathrm{NM_L} = V_{\mathrm{IL}} - V_{\mathrm{OL}}. \tag{2}$$

IV. Discussion

V. Conclusion