

Homework 9 - Aidan Sharpe

Problem 1

Find the best width and spacing to minimize the RC delay of a metal2 bus in a 180[nm] process if the pitch cannot exceed 960[nm]. Minimum width and spacing are 320[nm]. First, assume that neither adjacent bit is switching. How does your answer change if the adjacent bits may be switching?

Not Switching

When the bits are not switching, the speed is dependent on minimizing R . R is smallest when w is largest. If s must be at least 320[nm] and $s + w$ must be no more than 960[nm], then the largest w can be is 640[nm]. Therefore, the optimal pair is $s = 320$ [nm] and $w = 640$ [nm].

Switching

When the bits are switching, the speed is dependent on minimizing the time constant RC . Estimating the value for C from Figure 6.12, yields $s = 480$ [nm] and $w = 480$ [nm] to be optimal for minimizing the delay for switching bits.