VLSI Exam 1

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Question 1

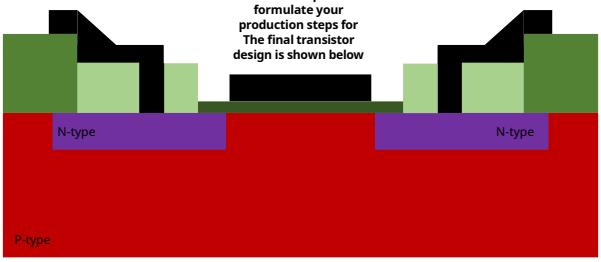
a) A gate would not be designed with poly because of its high resistance, this causes it to both consume more energy than other materials and produce more heat. Heat is difficult to manage is one of the constraints when decreasing the size of transistors.

Aluminum is not widely used for the gate, source, and drain of transistors currently, as while it offers significantly lower resistance than polysilicon, it can alloy with silicon during high temperature steps of the manufacturing process and cause internal short circuits. The temperatures used during the production process are also very often higher than the melting point of aluminum which complicates manufacturing.

b)

nMOS Transistor with Aluminum Gate Fab Process

Exam Prob. # 1
Use this template to formulate your production steps for The final transistor design is shown below



1

Legend

- P-type Silicon
- Silicon Oxide
- Photo Resist
- N-type Silicon
- Chrome Mask
- Aluminum

Use this for depicting etching

2

Blank Wafer

A p-type wafer is used as the basis of the nMOS

Legend
P-type Silicon
Silicon Oxide
Photo Resist
N-type Silicon
Chrome Mask
Aluminum

3

Grow SiO2 on top of Si wafer

A layer of SiO2 is grown at 900-1200 degrees C with either water or pure oxygen in the furnace

Legend
P-type Silicon
Silicon Oxide
Photo Resist
N-type Silicon
Chrome Mask
Aluminum

4

Spin on Photoresist

Photoresist is applied over the layer of SiO2

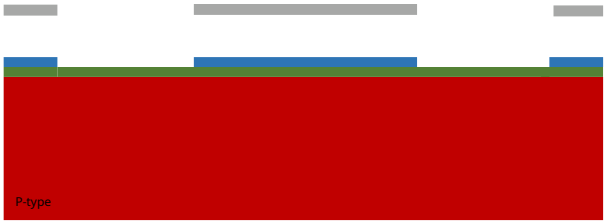
Legend
P-type Silicon
Silicon Oxide
Photo Resist
N-type Silicon
Chrome Mask
Aluminum

5

Mask and Expose Photoresist

When light is shone onto photoresist through holes in a mask it becomes softer

Legend
P-type Silicon
Silicon Oxide
Photo Resist
N-type Silicon
Chrome Mask
Aluminum



6

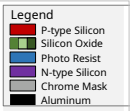
Oxide Etch

The softer photoresist is then strippped off and the SiO2 is etched with hydrofluoric acid
The photoresist ensures that only the portion of SiO2 with the photoresist removed is etched

7

Strip Photoresist

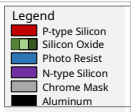
The photoresist is then completely removed using a combination of acids called piranah etch



8

Ion Implantation or Diffusion

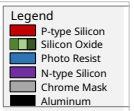
The wafer is then either placed into a furnace with arsenic gas and heated until the arsenic atoms diffuse into the exposed SiO2 or blasted with arsenic ions



9

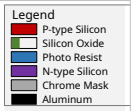
Strip oxide

All of the SiO2 is then removed



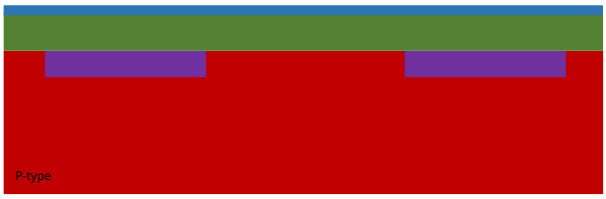
10

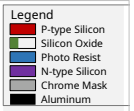
Grow Thick Oxide



11

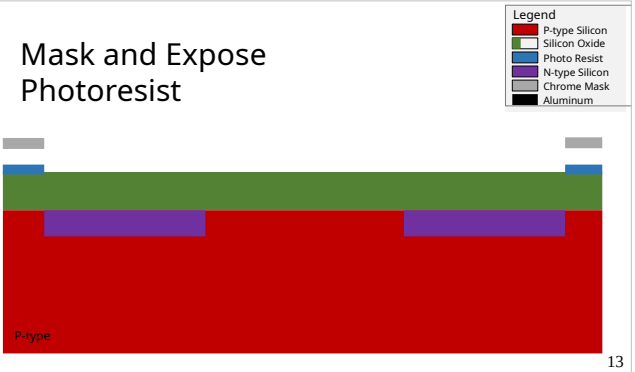
Spin on Photoresist





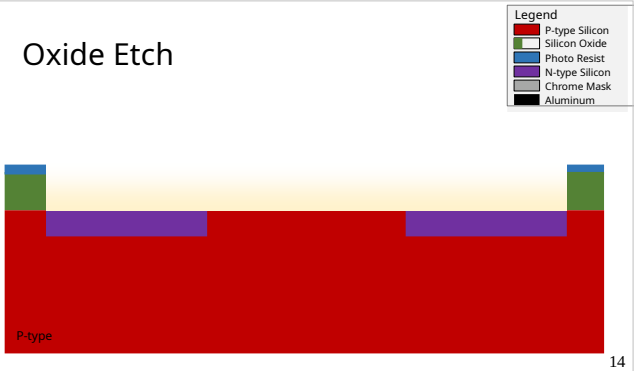
12

Mask and Expose Photoresist



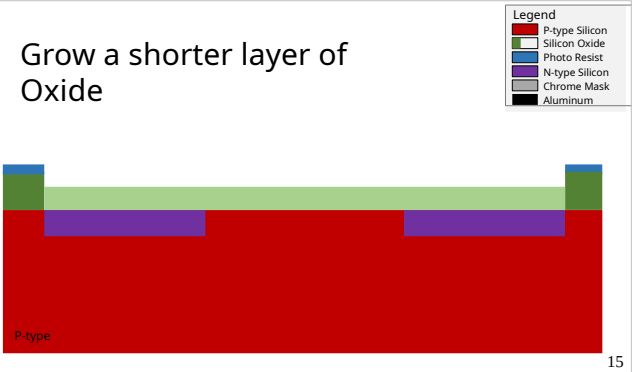
13

Oxide Etch



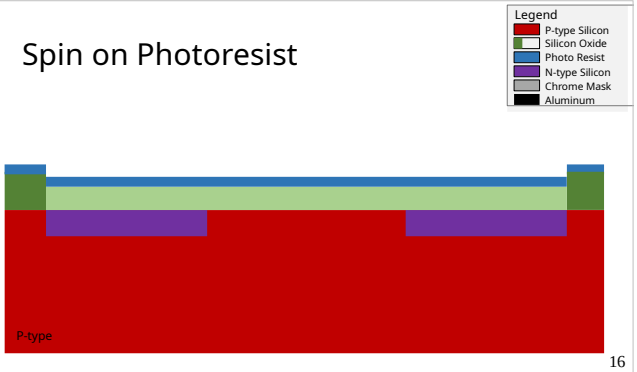
14

Grow a shorter layer of Oxide



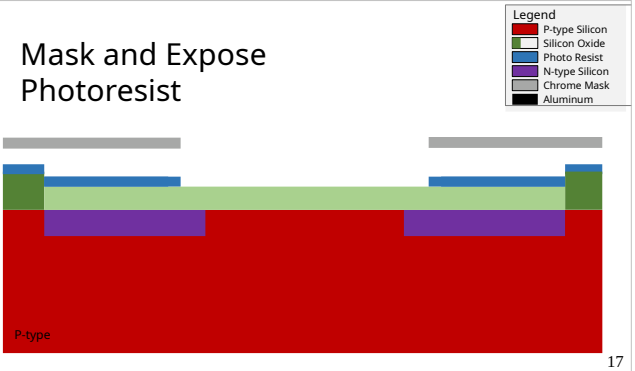
15

Spin on Photoresist



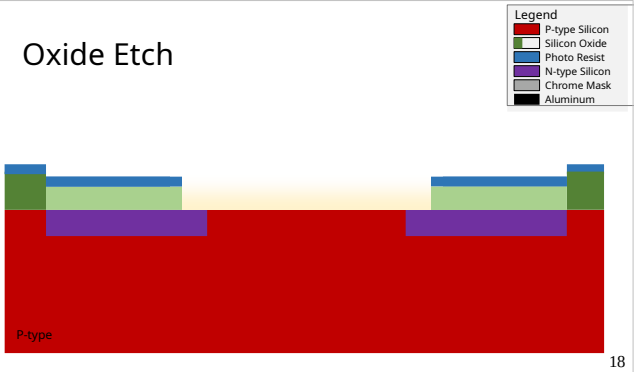
16

Mask and Expose Photoresist



17

Oxide Etch



18

Grow a thin layer of oxide

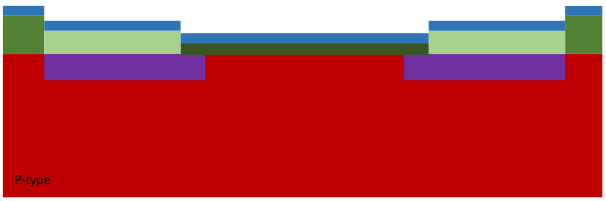
A very thin layer of oxide (20 Angstroms thick) is then grown to form the gate oxide of the transistor

19

Strip Photoresist

20

Spin on Photoresist



21

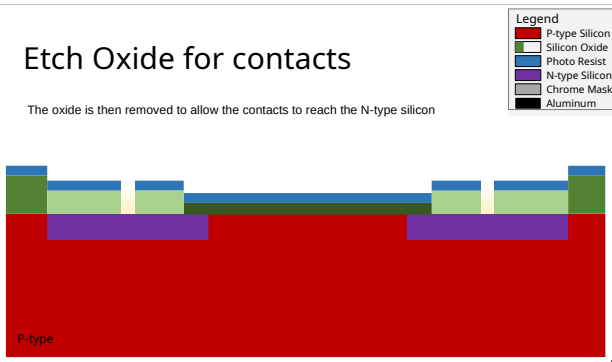
Mask and Expose Photoresist

A final exposure of photoresist is done to create holes in the SiO2 for the contacts

22

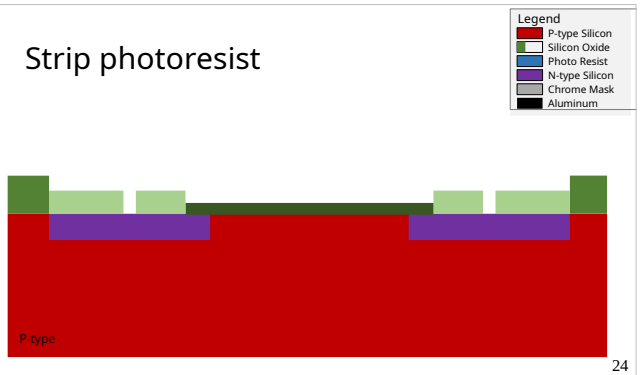
Etch Oxide for contacts

The oxide is then removed to allow the contacts to reach the N-type silicon



23

Strip photoresist



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Add Aluminum

Aluminum is now sputtered onto the wafer with a pattern placed over it to ensure that the aluminum is only applied where needed

List of steps – not in order

This a list of representative production steps for making a transistor. These are not in order, but I can say that each step will be used at least once with most being used multiple times throughout the design process.

- Ion Implantation or Diffusion
- Add Aluminum
- Photoresist
- Grow Oxide
- Grow a shorter layer of Oxide
- Grow a thin layer of Oxide
- Grow Thick Oxide
- Oxide Etch
- Etch Oxide for contacts
- Mask and Expose
- Strip Photoresist
- Strip Photoresist then all Oxide

Question 2

$$\begin{array}{cc} L_n = 0.6\mu\text{m} & L_p = 0.6\mu\text{m} \\ K_n = 122\mu A/V^2 & K_p = 61\mu A/V^2 \\ V_{TN} = 0.7V & V_{TP} = -0.7V \end{array}$$
$$C_{ox} = 33 \times 10^{-4}\text{pf}/\mu\text{m}^2$$
$$K = \mu C_{ox}$$

A)

$$V_{gs} = V_{ds} = 5V$$

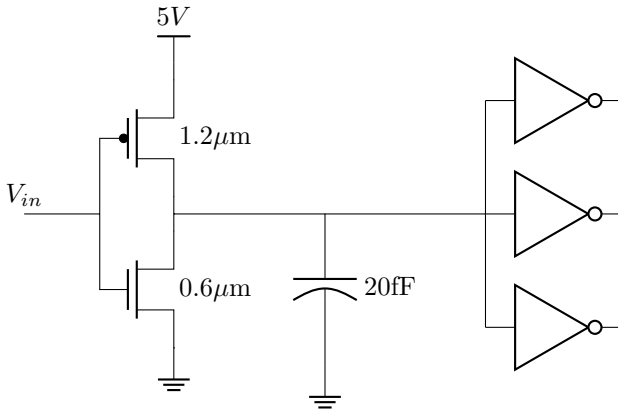
$\therefore$ The transistor is in saturation

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{gs} - V_T)^2$$
$$2.82 \times 10^{-3} = \frac{1}{2} \times \frac{W_n}{0.6\mu\text{m}}(5 - 0.7)^2$$
$$W_n = 1.5\mu\text{m}$$

B)

$$2 = \frac{W_p}{W_n} = \frac{W_p}{1.5\mu\text{n}}$$
$$W_p = 3\mu\text{m}$$

C)



From the textbook: $C_g = C_{sb} = C_{db}$

$$C_g = C_{ox}WL = C_{ox}WL$$
$$C_{g,n} = 33 \times 10^{-4}(1.5)(0.6) = 2.97\text{fF}$$
$$55.64\text{fF} = 12(2.97\text{fF}) + 20\text{fF} \text{ (Found using circuit from part D.)}$$
$$\beta = K'\frac{W}{L}$$
$$\beta_n = 122\frac{1.5}{0.6} = 305\mu A/V^2$$

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \\ \beta(V_{gs} - V_t - V_{ds}/2)V_{ds} & V_{ds} < V_{gs} - V_t \\ \frac{\beta}{2}(V_{gs} - V_t)^2 & V_{ds} > V_{gs} - V_t \end{cases}$$

$$I = C\frac{dv}{dt}$$

Saturation:

$$I = 2.82mA(\text{Given})$$

$$0.00282 = 55.64 \times 10^{-15}\left(\frac{0.7}{dt}\right)$$

$$\Delta t = 13.81\text{ps}$$

Linear:

$$v\,(t) = V_o e^{-t/RC}$$

$$\frac{dv}{dt} = \frac{-e^{-t/RC}V_o}{RC}$$

$$I = C\frac{dv}{dt}$$

The current is negative as the capacitor is discharging

$$-I = C\frac{-e^{-t/RC}V_o}{RC}$$

Substituting in $I = 2.82$mA, $R = 10$k, $C = 55.64$fF, and $V_o = 5$V for the edge of the linear region finds $t = 15.9404$ns. Then substituting $I = 0.612$mA for the current at 0.5V finds $t = 16.7853$ns. Subtracting these gives a $\Delta t = 845$ps and adding the delay from the saturation region gives a discharge time of $t = 858.81$ps.

D)

i. Stick Diagram and Layout

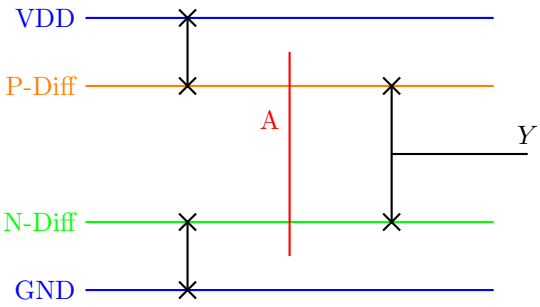


Figure 1: Inverter Stick Diagram

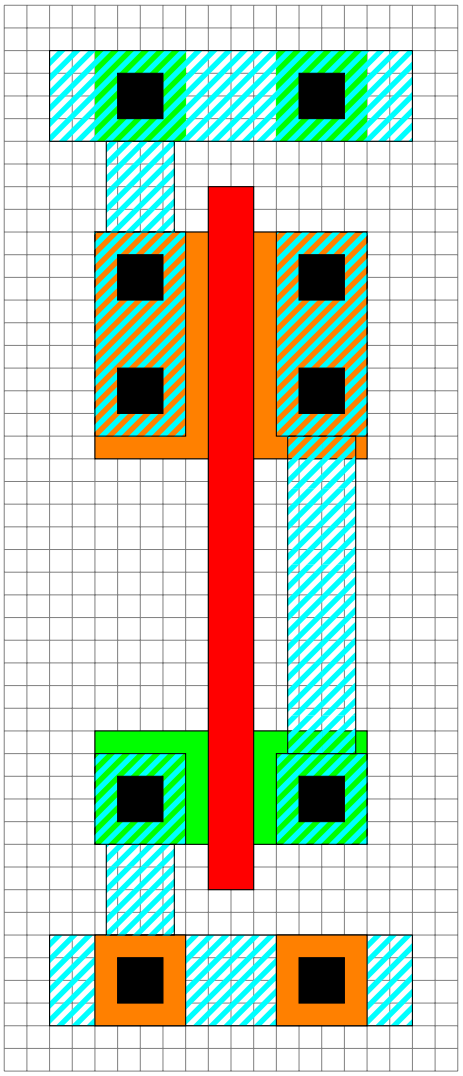
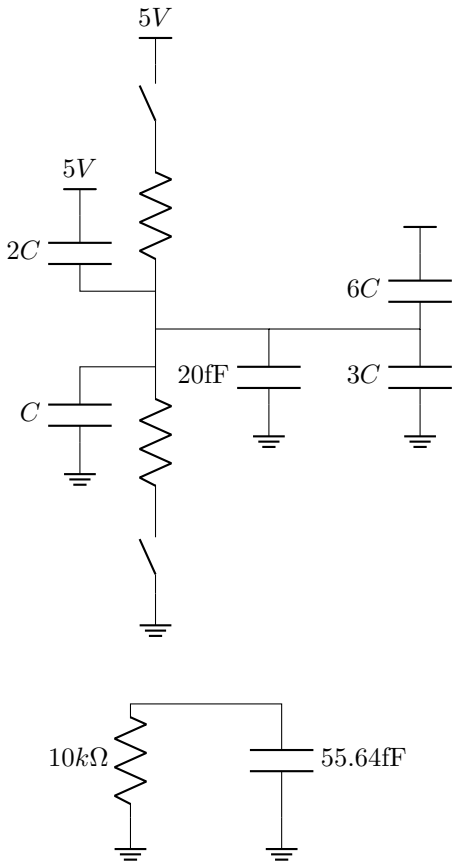


Figure 2: Inverter Layout (Grid = 1λ)

ii. Using the capacitances previously found:



Using $R = 10k\Omega$

$$t_{pdf} = (10k\Omega)(55.64\text{fF})\ln(2) = 385.667\text{ps}$$
$$t_{pdr} = (10k\Omega)(55.64\text{fF})\ln(2) = 385.667\text{ps}$$
$$t_{pd} = \frac{t_{pdf} + t_{pdr}}{2} = \frac{385.667\text{ns} + 385.667\text{ps}}{2} = 385.667\text{ps}$$

iii. From the Cadence analysis, $t_{pdf} = 283$ps and $t_{pdr} = 198$ps. The simulation was conducted as a transient simulation with pulse input with a period of 2ns, rise and fall times of 0.1ns, a "high" time of 1ns, a "low" voltage of 0 volts, and "high" voltage of 5 volts. $\therefore t_{pd} = 241$ps.

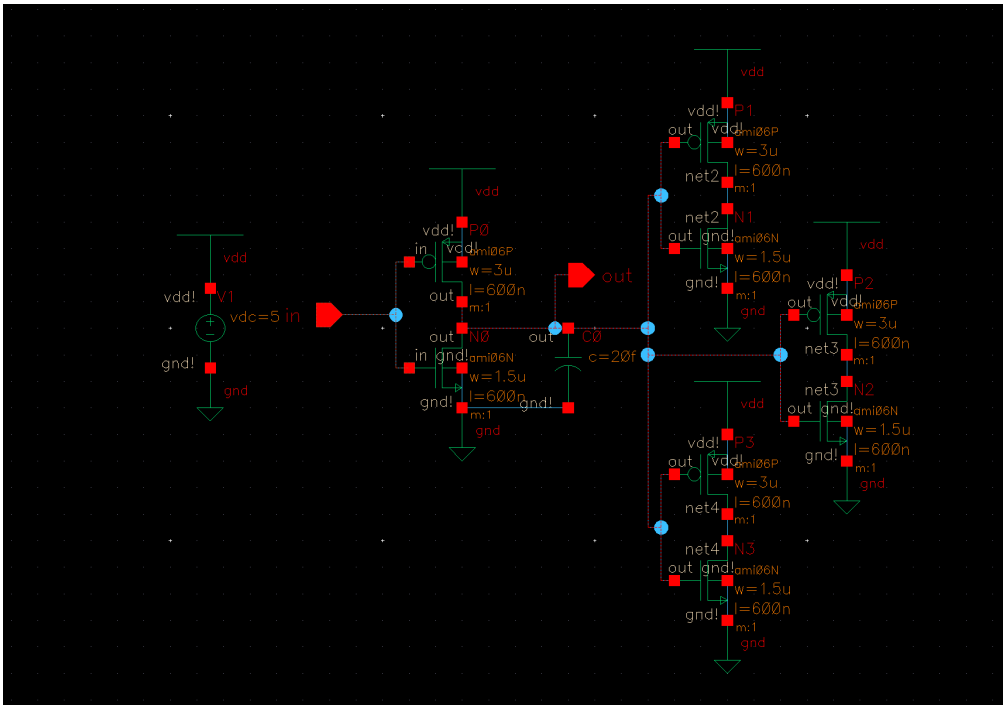


Figure 3: Cadence Schematic

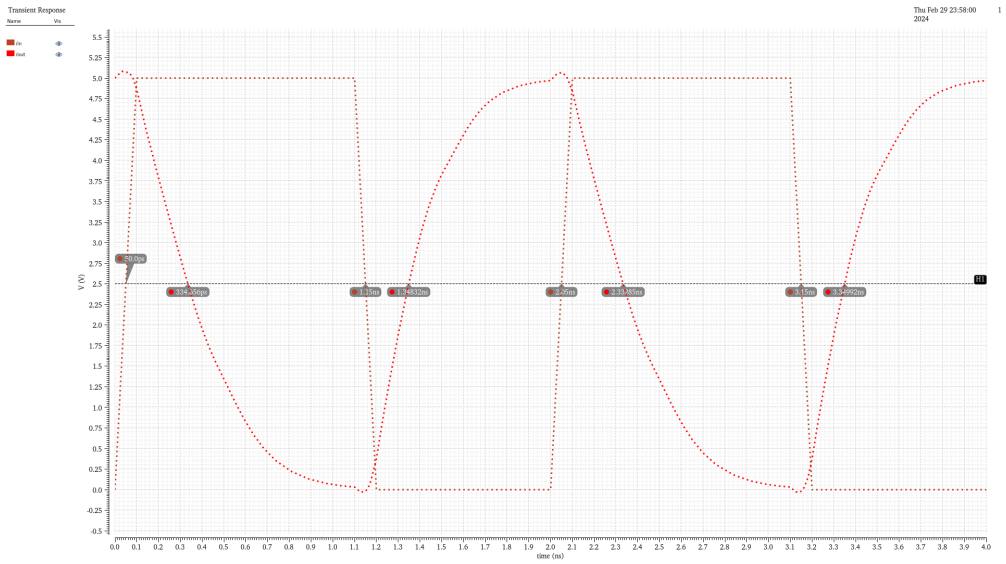


Figure 4: Cadence Simulation Results

iv. The difference between the values obtained from Cadence and the values calculated in the previous part is like due to the assumptions that are made. The resistance of $10K\Omega$ used for the RC Time Delay Model is likely not as accurate as the values Cadence uses, nor is the RC time delay model the most accurate method for estimating delay. The capacitances used for the RC Time Delay model are also not as accurate as those used by Cadence, as it was assumed that $C_g = C_{sb} = C_{db}$. The Shockley Model was the least accurate by a significant amount due to the large number of factors and transistor properties that it ignores.

```
// Point Netlist Generated on: Mar  1 15:37:17 2024
// Generated for: spectre
// Design Netlist Generated on: Feb 29 23:53:31 2024
// Design library name: Exam1
// Design cell name: invx
// Design view name: schematic
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global 0 vdd!
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include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06P.m"

// Library name: Exam1
// Cell name: invx
// View name: schematic
P3 (net4 out vdd! vdd!) ami06P w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u \
        pd=9u m=1 region=sat
P2 (net3 out vdd! vdd!) ami06P w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u \
        pd=9u m=1 region=sat
P1 (net2 out vdd! vdd!) ami06P w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u \
        pd=9u m=1 region=sat
P0 (out in vdd! vdd!) ami06P w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u pd=9u \
        m=1 region=sat
N3 (net4 out 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u pd=6u \
        m=1 region=sat
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        m=1 region=sat
N1 (net2 out 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u pd=6u \
        m=1 region=sat
N0 (out in 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u pd=6u \
        m=1 region=sat
V1 (vdd! 0) vsource type=dc dc=5
C0 (out 0) capacitor c=20f m=1
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finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
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