ECE 09.414 – Fall 2024
Exam 1 – Take Home – Due on 10/10/2024
100 Points
Prof. Fifth

You will submit your work on Canvas. In completing these questions, feel free to make reasonable assumptions but be sure to state them clearly and check them when possible.
Some rules:

- You are welcome to use any notes and/or books, however, you are not permitted to have the assistance of any other person on the exam.
- If you have any questions regarding interpretation of the questions, you should personally ask and/or send a message with your question through Canvas.
- Use one side of a page only for printed solutions.
- New problems start on a new page.
- Label all problem numbers and parts.
- Circle your answers.
- Show all steps, even the simple ones.

1) (25 Points) A typical MOSFET design, having the same structure as shown in Figure 1, uses Aluminum for the source, gate and drain material. Use the power point template provided to formulate the manufacturing process **(NO HAND DRAWINGS WILL BE ACCEPTED)**

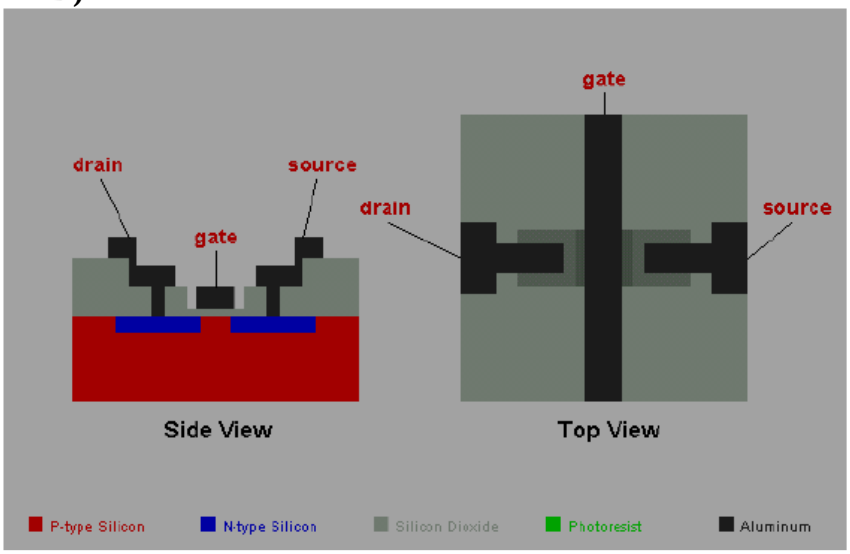

Figure 1

a. From discussions in class, for large scale production we would never design a gate with poly nor use aluminum for the source and drain. Do some research and discuss when it would be appropriate to use Aluminum for Gate, source and drain as depicted in Figure 1. (5 Points)

b. Make a process sequence (with pictures) for the fabrication of this structure including the lithography (mask) and removal steps (do not skip any steps). Briefly discuss the purpose of each mask step and discuss the specific conditions needed for that step (time, temp, thickness, etc…). (Hint: Keep in mind that Aluminum has a lower melting point than other materials including Metal 1 so you cannot just replace one material for another without changing the process steps. Also pay attention to the shape of the aluminum and what layer it is on; it cannot be laid out in one step.) (20 points).

2) Given (Figure 2):
L_n = 0.6 μm (NMOS), L_p = 0.6 μm (PMOS)
K'n = 122 μA / V^2 (where K = μC_{ox}), K'p = 61 μA / V^2, C_{ox} = 33 x 10^{-4} pf / μm^2
V_{TN} = 0.7 V, V_{TP} = -0.7 V
   a. (5 Points) Determine the width of an NMOS transistor which draws 2.82 mA of current between source and drain when its Vgs = Vds = 5 Volts.
      i. You have all the values needed to solve for w_n using the appropriate current equation.
   b. (2 Points) What is the corresponding W of the PMOS device if the gate is to have symmetrical delay characteristics?
      i. You can then use the ratio relationship between nmos and pmos to find wp.
   c. (18 Points) This NMOS transistor is used as the pull down of an inverter loaded by three similar CMOS inverters plus an interconnect capacitance of 20 fF. Calculate the time to discharge Vout from 5 Volts to 0.5 Volts using Shockley "simple" MOSFET models assuming a 0V to 5V step function input.
      i. (3) You need to find the input cap of the inverter and the fan-out load cap.
      ii. (3) Add your total load cap together, this includes the interconnect cap.
      iii. (12) To find the total delay you will need to break this problem up into the appropriate operating voltage ranges (time through saturation and another time through linear).
      Remember: $I = C(dv/dt)$, and $v(t) = V_0 e^{-t/RC}$
   d. (20 Points) Sketch an RC and Elmore delay model for a 3 input NAND (NAND3). Include both the pull-up and pull down network operations separately in separate circuit diagrams.
   e. (30 Points)
      i. (5 Points) Sketch a stick diagram and layout (to scale with the lambda sizes) for the inverter in figure 2 (I want both, you may need graph paper).
      ii. (10 Points) Sketch and estimate its delay using the RC time delay model (not Elmore), (you will need to find Cg in fF/um {ie cap per micron used in the final delay calculation} with the final delay using $R = 10k\Omega \cdot \mu m$).
      iii. (10 Points) Now use the Elmore delay model to calculate the timing delay for this circuit.
      iv. (5 Points) Compare the delay calculated using RC vs Elmore. Explain the reason(s) for any differences.

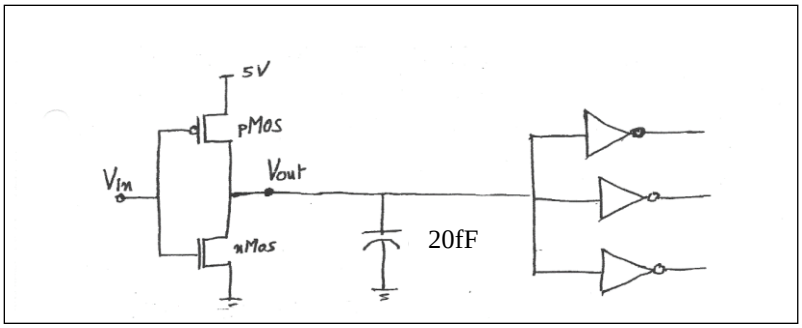

Figure 2