

VLSI Homework 10 - Aidan Sharpe

Problem 1

You are synthesizing a chip composed of random logic with an average activity factor of $\alpha = 0.1$. You are using a standard cell process with an average switching capacitance of $C_{\text{avg}} = 450[\text{pF}/\text{mm}^2]$. Estimate the dynamic power consumption of your chip if it has an area of $70[\text{mm}^2]$ and runs at $450[\text{MHz}]$ at $V_{DD} = 0.9[\text{V}]$.

$$P_{\text{dynamic}} = C_{\text{sw}}V_{DD}^2f_{\text{sw}}$$

```
alpha = 0.1           # Activity factor
C_avg = 450E-12       # Average switching capacitance [F / mm^2]
A = 70                # Chip area [mm^2]
f = 450E+6            # Clock frequency [Hz]
V_DD = 0.9            # Supply voltage [V]

C_sw = C_avg * A      # Total switching capacitance [F]
f_sw = alpha * f      # Switching frequency [Hz]

P_sw = C_sw * V_DD**2 * f_sw # Dynamic power [W]

print(f"Dynamic Power: {P_sw}")
```

$P_{\text{dynamic}} = 1.148175[\text{W}]$
