Project 2A - Clock Breadboard
ECE09402 - Rapid Prototyping and Fabrication

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March 14th, 2025

Introduction

The goal of this project is to prototype a single digit from a seven segment display-based digital clock. Once functionality is verified, the circuit will be adapted for a printed circuit board (PCB).

Design Requirements

1. Display brightness shall be the same regardless of the digit being displayed
2. The digit shall be incremented with a momentary switch
    a. The output of the momentary switch shall be debounced
3. The digit shall support rolling over from 9 to 0
4. The digit shall also support rolling over from 5 to 0
5. The display shall be an INND-TS30RCB
6. The display shall be driven with a CD4026BE decade counter
7. The design shall utilize a CD4073BE three-channel, three-input AND gate

Results

The final breadboard layout configured for rolling over from 5 to 0 is seen in the figure below. The wire colors represent the following:

- Red: +5v
- Black: ground
- Purple clock input
- Yellow: roll over logic inputs to the AND gate (segments E, F, G)
- Blue: display driver and AND gate outputs
- White: button output

To switch to 9 to 0 roll over mode, the diode (highlighted as D1 below) should be removed, and the reset pin (pin 15) of the CD4026BE should be tied to ground (*CMOS Decade Counters/Dividers* 2003).
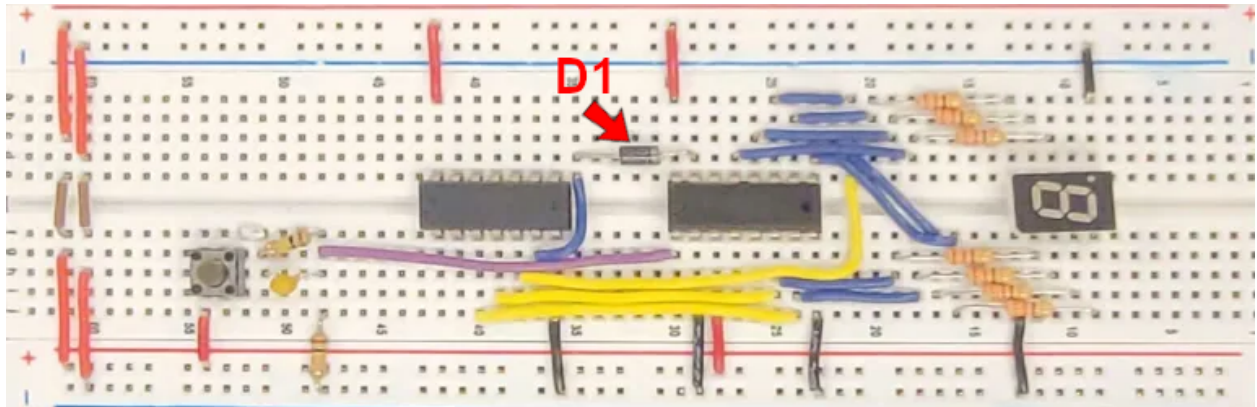

Figure 1: Final circuit top view

In this mode, the system was tested with a signal generator set up to output a 50% duty cycle, 1Hz, 5v square wave. The signal generator setup is seen below.

Momentary switches can bounce when pressed or released, which has the effect of multiple pulses. In the case of this design, the bouncing of the button will cause CD4026BE to count multiple times. This behavior is undesirable, but can be resolved with a de-bouncing circuit. The de-bounce circuit implemented is simply a low pass filter with a pull down resistor to discharge the capacitor. The final design is seen in figure 3.
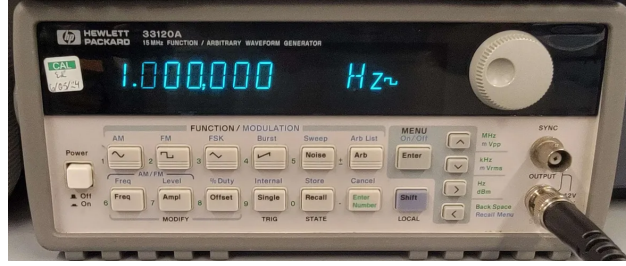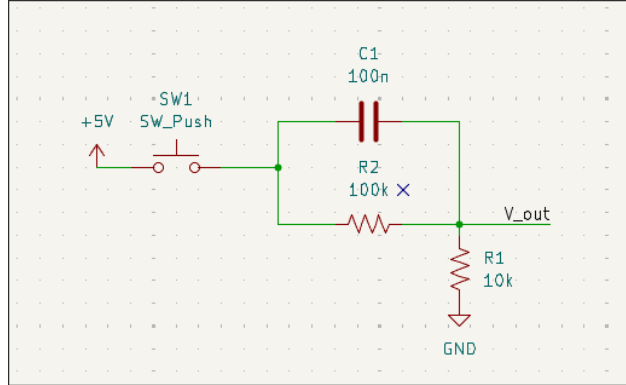
Figure 2: Signal generator setup

Figure 3: Debounce schematic

Reflection

Integrated circuits such as the INND-TS30 seven segment display with a 300mil spacing between the inline pins must be bent to fit into the breadboard (*INND-TS30 Series 0.3" Through Hole Single Digit Display* 2017). Bending the pins in this way makes it very easy for the IC to pop out or to make poor electrical contact with the breadboard.

Planning ahead is critical to breadboarding. In this case, I planned out the best orientations of the seven segment display with respect to its driver. Importantly, the pins on the driver (*CMOS Decade Counters/Dividers* 2003) are not in the same order or always on the same side of the IC as the display (*INND-TS30 Series 0.3" Through Hole Single Digit Display* 2017).

We also learned that sometimes devices do not behave as expected. The CD4073BE that was originally distributed was part of a faulty batch. The expected behavior is that when pins 11, 12, and 13 are logic high, pin 10 is also logic high (*CMOS AND Gates* 2003). During our testing, we noticed that the faulty chips did not exhibit this behavior, with the output remaining low regardless of the input state. Unfortunately, these issues are difficult to debug and can really only be remedied with a different batch of parts.

Finally, we learned that there are a lot of first order RC low-pass filter topologies for the debounce circuit. We used the design in figure 3 as it debounced on both the rising and falling edges. The initial design we implemented only debounced the falling edge, but during testing, the rising edge would sometimes trigger multiple clock pulses.

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References

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